Lecture Outline

- From reader

- Today’s Lecture
  - Hurdles and benefits of process integration
  - Modular processes
    - CMOS before MEMS
    - MEMS before CMOS
  - Interleaved processes
  - MEMS by foundry CMOS
Types of Integration

Integrated Monolithic MEMS

- Motivation for co-fabrication
  - Improved device performance, higher signal-to-noise ratio
  - Reduced size, power requirement
  - IC compatibility = economical manufacturing
  - Automatic alignment; packaging combined

<table>
<thead>
<tr>
<th>Common features</th>
<th>CMOS</th>
<th>Surface Micromachining</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process Flow</td>
<td>Standard</td>
<td>Application specific</td>
</tr>
<tr>
<td>Vertical Dimension</td>
<td>~1 µm</td>
<td>~1-5 µm</td>
</tr>
<tr>
<td>Lateral Dimension</td>
<td>&lt;1 µm</td>
<td>2-10 µm</td>
</tr>
<tr>
<td>Complexity</td>
<td>&gt;10 masks</td>
<td>2-6 masks</td>
</tr>
</tbody>
</table>
**Thermal Budget**

- Critical temperatures for Al metallization
  - Degradation at $T > 400-450^\circ C$
  - Junction migration at $T = 950^\circ C$
  - Junction spiking

- Critical process temperatures for MEMS

<table>
<thead>
<tr>
<th>Temperature</th>
<th>Material</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPCVD</td>
<td>LTO/PSG</td>
</tr>
<tr>
<td>450°C</td>
<td>Low stress polySi</td>
</tr>
<tr>
<td>610</td>
<td>Doped polySi</td>
</tr>
<tr>
<td>650</td>
<td>Nitride</td>
</tr>
<tr>
<td>800</td>
<td></td>
</tr>
<tr>
<td>Annealing</td>
<td>PSG densification</td>
</tr>
<tr>
<td>950</td>
<td>PolySi stress annealing</td>
</tr>
<tr>
<td>1050</td>
<td></td>
</tr>
</tbody>
</table>

*W. Yun, PhD Thesis, BSAC*

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**Benefits and Hurdles**

- **Benefits to integration**
  - Lower parasitic capacitance and parasitic resistance, greater sensitivity
  - Increased reliability, reduced size and package complexity

- **Challenges to integration**
  - MEMS layer deposition and anneal temperatures
  - Passivation of CMOS during MEMS etching and release steps
  - Surface topography of MEMS
  - Materials incompatibilities
  - Yield losses multiplied
  - Special purpose electronics may be needed
This Lecture

• Modular processes
  • CMOS before MEMS
    • UC Berkeley Modular Integration
    • UCB polysilicon germanium
    • SOI MEMS, UCB and Analog Devices
  • MEMS before CMOS
    • Sandia Labs MM/CMOS

• Interleaved CMOS and MEMS
  • Analog Devices BiMEMS
  • Bosch epipoly

• MEMS by CMOS foundry
  • Parameswaran et al., University of Alberta, 1988
  • Fedder et al., Carnegie Mellon, 1996

Modular Processes

• CMOS before MEMS
  + IC foundry can be used
  + Chip area may be minimized
    – Thermal budget is an issue

• MEMS before CMOS
  + No thermal budget for MEMS
    – Microstructure topography is an issue
    – Electronics and MEMS cannot be easily stacked
    – IC foundries are wary of pre-processed wafers (materials constraints)
UCB Process

- Refractory metallization (e.g. tungsten), makes possible high-temperature post-processing
- Double-poly, single-metal CMOS, passivated with PSG
- Low-stress nitride for protection from release etch
- MEMS-CMOS interconnect: MEMS ground plane doped poly to CMOS gate poly

Issues

- Tungsten, W, reacts with Si at 600°C to form WSi₂ → diffusion barrier is needed; e.g. TiN/TiSi₂

Problems

- W forms hillocks during annealing, relatively high contact resistance
- Mainstream CMOS processes are optimized for Al (now Cu)
- Heavily doped MEMS layers can affect CMOS
Polysilicon Germanium

- Poly-Si$_{1-x}$Ge$_x$
  - Low temperature, Low resistivity with doping
  - n-type poly-Ge structural; SiO$_2$ sacrificial
  - p-type poly-Si$_{0.35}$Ge$_{0.65}$ structural; poly-Ge sacrificial

- Deposition
  - LPCVD thermal decomposition of GeH$_4$ and SiH$_4$ or Si$_2$H$_6$
  - Rate >50 Å/min, T < 475°C, P = 300-600 mT
  - At higher [Ge]: rate ↑, T ↓
  - In-situ doping, ion implantation

- Dry etching
  - Similar to poly-Si; F, Cl, and Br-containing plasmas
  - Rate ~ 0.4 µm/min

- Wet etching
  - H$_2$O$_2$, 90°C: 4 orders of magnitude selectivity between >80% and <60% Ge content.
  - Good release etchant

Fig. 2. Etch rate of poly-Si$_{1-x}$Ge$_x$ films in RCA SC-1, and hydrogen peroxide.

J. Heck PhD thesis, Howe and King groups
Poly-SiGe Mechanical Properties

- Conformal deposition
- Low stress as-deposited
- Films have high roughness
- Young’s modulus ~146 GPa (poly-Si$_{0.35}$Ge$_{0.65}$)
- Fracture strain 1.7% (compared to 1.5% for MUMPS polySi)
- Q = 30,000 for n-type poly-Ge in vacuum
- Poly-SiGe mechanically on par with poly-Si

UCB Poly-SiGe Process

- 3 µm standard CMOS process, Al metallization
- p-type poly-Si$_{0.35}$Ge$_{0.65}$ structural; poly-Ge sacrificial
- MEMS-CMOS interconnect through p-type poly-Si strap
- Process:
  - CMOS passivated with LTO, 400°C
  - Vias to connection strap opened
  - Ground plane deposited, MEMS built.
  - RTA anneal to lower resistivity (550°C, 30s)
Integrated SOI MEMS

- To increase resolution of inertial sensor
  - Reduce spring stiffness
  - Increase proof mass

\[ F = ma \]
\[ F = kx \]
\[ x = \left( \frac{m}{k} \right) a \]

- Silicon-on-insulator integrated process
  - MEMS 25\( \times \) thicker than with poly surface micromachining
  - SCS MEMS: zero stress and stress gradient
  - Integration of high sensitivity structures with circuitry gives 5-25\( \times \) better resolution

SOI MEMS Process

- Trench (2 \( \mu \)m wide) encloses future MEMS region
- Insulating silicon nitride fills trench
- Silicon nitride etched back from wafer surface
- Standard CMOS made and interconnected to future MEMS by metal or doped poly
- MEMS structures defined using deep etch
- Buried oxide etched to release MEMS
### SOI Accelerometer Parameters

- **Chip size**: 3.4 × 2.9 mm$^2$
- **Sensor size**: 1 × 1.5 mm$^2$
- **Proof mass**: 52 µg
- **Resonant frequency**: 3 kHz
- **Sense capacitance**: 9.7 pF
- **Full scale**: ±1.75 g
- **Power consumption**: 5 V × 5 mA
- **Sensitivity**: 102 fF / g
- **Noise floor**: 25 µg / √Hz
- **On-chip A/D conversion**
Sandia Embedded Process

1. Trench etched into Si using KOH
2. MEMS fabricated in trench
3. Trench filled with LPCVD oxide
4. Trench planarized with CMP
5. MEMS stress anneal
6. Trench seal with LPCVD nitride
7. Standard CMOS fabrication next to MEMS
8. CMOS passivated with PECVD nitride
9. Trench opened, MEMS released
Sandia Embedded Process

- 3 axis accelerometer
  - $4 \times 4 \text{ mm}^2$ chip
  - 3 proof masses to capacitively measure acceleration
    - X, Y: comb finger array
    - Z: parallel-plate capacitor
  - Each sensor has own interface circuitry
  - Differential circuitry allows sensing of fractions of attoFarad changes in capacitance
  - Measures up to $\pm 25 \text{ g}$

Interleaved and Foundry Processes

- CMOS and MEMS mixed
  + More control over materials, processes
  ± Optimize or compromise mechanical and electrical components
    – Need your own fab

- Foundry processes
  + Economical, reliability and yield high
  + Simple post processing step releases MEMS
    – Cost of increased chip area
    – Mechanical properties of CMOS layers compromised
Analog Devices BiMEMS Process

- ADXL50 accelerometer
  - Interleaved MEMS and 4 µm BiMOS fabrication
  - MEMS-CMOS interconnect by diffused n+ runners
  - Relatively deep junctions allow for MEMS poly stress anneal
  - Acceleration to volt transducer
  - Measurement of ±50 g accelerations

ADXL50 Specifications

- Chip size 3 × 3 mm² 3.4 × 2.9 mm²
- Sensor size 0.6 × 0.7 mm² 1 × 1.5 mm²
- Proof mass 0.28 µg 52 µg
- Resonant frequency 12 kHz 3 kHz
- Open-loop displacement 1.7 nm/g
- Sense capacitance 120 fF 9.7 pF
- Full scale ±5 g ±1.75 g
- Shock survival 1000 g
- Power consumption 5 V x 8 mA 5 V x 5 mA
- Sensitivity 200 mV/g 102 fF/g
- Noise floor 0.6 mg/√Hz 25 µg/√Hz
**ADXL202**

- ±2 g accelerations
- X and Y variable capacitors on sides of same larger proof mass
- Spring suspension minimizes cross-axis sensitivity
- Digital output (vs. ADXL50)

**Bosch Epi-Poly Process – 1**

- Buried layer defined
- Sacrificial oxide deposited, removed in circuit area and at MEMS anchor points
- Epitaxial deposition, 10µm
  - Monocrystalline above circuit area
  - Polycrystalline above oxide
  - At anchor points, SCS pyramids formed with (111) walls embedded in epipoly
- Surface is planar

Offenberg et al.

Bosch
**Bosch Epi-Poly Process – 2**

- Gate poly patterned
- Doping of gate and MEMS poly
- Dopant drive-in by annealing
- Standard BiCMOS process resumed, ending with metallization and passivation
- Trench etch epipoly structures
- Release using sacrificial oxide etch with HF vapor phase

**Bosch Results**

- As-deposited epipoly has low stress (<4 MPa), negligible stress gradient, and rough surface.
- 10 µm thick epipoly gives stiffness in z-direction
- Range ±35g
- Sensitivity 20 mV/g
Integrated MEMS by Foundry CMOS

- Fabricate using foundry CMOS
  - Unconventional layout designs
  - Unaltered process sequence
  - Single postprocessing step: isotropic or anisotropic etching
  - Only need to know CMOS design rules vs. processing details
  - Mechanical properties compromised

- History
  - Univ. Alberta 1988 (KOH), Cornell 1992 SCREAM process, UCLA 1995 (XeF₂), ETH Zurich 1990s, CMU 1996 ASIMPS process (SF₆)

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Integrated MEMS by Foundry CMOS

- Process
  - Laminated metal/insulator MEMS
  - Made using HP 0.8µm, 3-metal CMOS process at MOSIS foundry
  - Top metal layer used as etch mask for CHF₃/O₂ oxide etch
  - Final SF₆ isotropic etch releases structures

- Features
  - Independent electrostatic actuation possible due to multiple insulated metal layers

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Thermally isolated heater element
Parameswaran et al.
Univ. of Alberta

G. Fedder et al.
Foundry 1

Integrated MEMS by Foundry CMOS

- Accelerometer parameters
  - Range \( \pm 13 \) g
  - Out-of-plane curl 6 \( \mu m \)
  - Displacement 3.1 nm / g
  - Q 1200
  - Noise floor 1 mg/\( \sqrt{\text{Hz}} \)

Courtesy Gary Fedder, Carnegie-Mellon University

Foundry 2

MEMSIC Accelerometer

- MEMSIC (Andover, Mass.) dual-axis thermal accelerometer
- Post-foundry CMOS dry bulk micromachining to form thermal isolation cavity
- Sensor consumes large fraction of total chip area \( \rightarrow \) cost of adding “accelerometer function” still high, even if post-process steps are very simple and high-yield
Summary

• CMOS first
  • State-of-the-art CMOS foundries can be used
  • Thermal budget of metallization to be accounted for

• MEMS first
  • No thermal budget to worry about
  • Possible materials incompatibilities (high dopant structural layers, piezoelectrics)
  • Topography to overcome

• Interleaved
  • Potentially greater control over process steps
  • First commercially proven integrated process
  • Possibly compromises both CMOS and MEMS