Lecture Outline

• Reading

• Problem set #2 on website, due next Tuesday 9/16

• MUMPS Labs after class: 4-5, 5-6 pm
  • Where Prof. Howe’s grad students demonstrate MUMPS devices and you help…
  • 6-10 students per session

• Today’s Lecture
  • MEMS Test Structures for Film Characterization (from Lecture 4)
  • Stiction and Friction in MEMS (from Lecture 4)
  • 3-D Microstructures
Lecture Outline

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- Approaches
  - Hinges
  - Molding: Hexsil
  - Silicon-on-Insulator Process
  - Sealed-cavity Deep RIE Process
  - SCREAM

Hinge Process Flow

Deposit first sacrificial
Deposit and pattern first poly

Pattern contacts
Deposit and pattern second poly

Deposit and pattern second sacrificial
Etch sacrificial
Assemble part

Pop-Up MEMS

First MEMS hinge, K. Pister, et al. 1992

Corner Cube Reflector: V. Hsu, 1999

Hinged Campanile made in SUMMiT process, assembled using probes Elliot Hui et al.
Assembling Hinges

• Assembly using
  • Grad students’ eyebrows!
  • Fluidic agitation
  • On-chip actuators
  • Magnetic forces
  • Surface tension of precisely located droplets

Deformable Hinges and Flexures

• Flexible hinges
  • Rigid polySi plates (E = 140 GPa) connected by elastic polyimide hinges (E = 3 GPa), Suzuki et al.
  • Aluminum hinges fabricated in standard CMOS process, released with XeF₂, Pister et al.

• Pop-up flexures
  • Nickel film has tensile stress
  • Nickel-polySi “bimorph” legs
Molding Hexsil

- Makes high aspect ratio structures using conformal thin films in mold trenches
- Parts are demolded (and transferred to another wafer)
- Mold can be reused
- Honeycomb structure

Hexsil MEMS

Heck, Muller and Howe

MEMS Precision Instruments
Silicon on Insulator Process

- Silicon-on-Insulator (SOI) wafer
  - Thin layer of SCS (10's of nm – 10's of µm) on oxide layer (few 100's of nm) on handle Si wafer
    - SIMOX
    - Bonded SOI
  - CMOS compatible
  - Cost: ~$200 per wafer
- Fabrication
  - Dry etching to pattern Si layer
  - Etch buried SiO₂ to release

SOI Process

- SOI starting material
- Trench and Backfill
- Integrated Circuitry
- Structure definition and release

Proof mass 52 µg

Brosnihan et al.

Analog Devices

Lemkin et al.
Sealed-cavity Deep RIE Process

- Si substrates are polished to desired thickness, micromachined, and fusion-bonded together in a stack.