LOCALIZED SYNTHESIS OF SILICON NANOWIRES

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ABSTRACT

Localized resistive heating of microstructures has been used to activate vapor-deposition synthesis of silicon nanowires in a room-temperature chamber. The process is localized, selective, scalable and compatible with on-chip microelectronics and, in addition, removes necessity of post-synthesis assembly of nanowires to accomplish integrated nano-electromechanical systems. Synthesized nanowires with dimensions of 30-80 nm in diameter and up to 10 µm in length have been successfully demonstrated and growth rates of up to 1 µm/min have been observed. This new class of manufacturing method enables direct integration of nanotechnology with larger-scale systems for potential sensing and actuation applications.

INTRODUCTION

The unique electrical, mechanical and optical properties of nanowires have made them extremely attractive for a variety of applications [1-3]. However, a significant obstacle in the utilization of these nanostructures has been the difficulty in handling, maneuvering, and integrating them with microelectronics to form a complete system [3-5]. In addition, current synthesis processes for silicon nanowires require high temperature furnaces that could damage pre-existing microelectronics.

A novel scheme is presented here that allows for synthesis of silicon nanowires at a pre-specified location while eliminating the requirement of later assembly processes. Furthermore this occurs in a room temperature chamber. This localized and selective synthesis process is useful for direct integration of silicon nanowires with larger-scale systems, such as foundry-based microelectronics processes, including CMOS. The unique approach is based on localized resistive heating of suspended microstructures in a room temperature chamber to activate silicon nanowire synthesis via the vapor-liquid-solid (VLS) growth mechanism. The process described in this work is designed to take advantage of this mechanism.

EXPERIMENTAL

Two different types of suspended MEMS (Microelectromechanical Systems) structures were fabricated to serve as resistive microheaters for the synthesis processes: polysilicon microstructures fabricated using a standard surface micromachining process [6] and single crystal silicon (SCS) microstructures based on a silicon on insulator (SOI) wafer technology [7]. Figure 1(a-c) briefly illustrates the MEMS platform fabrication process. In both cases the microstructures were heavily doped with phosphorus and suspended 2 µm, as defined by the sacrificial silicon dioxide layer, above a silicon substrate for electrical and thermal isolation. The typical thickness of the bridges is 2 µm for polysilicon microstructures and 20 µm for SCS microstructures. A wet chemical oxide etching process naturally creates recessed regions underneath the electrical contacts such that the subsequent maskless catalyst deposition process in Fig. 1(d) cannot cause an electrical short-circuit. As necessitated by the VLS mechanism, a catalyst layer, approximately 5 nm thick, of a 60% gold - 40% palladium (AuPd) mixture was first sputtered on the surface of the released microstructures [8] as shown in Fig. 1(d). After attachment to a circuit board with electrical wire bonding process in Fig. 1(e), the microstructures were placed into the room temperature vacuum chamber. Figure 2 illustrates the experimental set up. The vapor phase, silane (10% SiH4 - 90% Ar) was introduced at 350 mTorr and the microbridge was resistively heated to initiate the silicon nanowire synthesis process.

It is believed that the VLS synthesis process can occur only under the right experimental conditions of temperature, gas pressure and suitable catalyst. The VLS mechanism was first proposed in the 1960s to describe whisker growth [9] and recently has been confirmed as responsible for nanowire growth [10]. In the context of silicon nanowires, the VLS reaction proceeds when silicon...
from the decomposition of silane interacts with the catalyst’s surface. The silicon diffuses into the catalyst; upon reaching the silicon-catalyst eutectic point, the alloy becomes liquid phase [10-11]. Various metallic catalysts (Ni, Fe, Ti, Zn, Au and AuPd [8, 9,12-15]) have been shown to effectively facilitate this reaction, with gold most commonly used. The liquid alloy continues to absorb silicon until it becomes supersaturated and silicon begins to precipitate at the liquid-solid interface [10-11]. Nanowires form as a result of this axial precipitation process. Since precipitation occurs at the solid-liquid interface, a catalyst nanoparticle present at the free tip of the nanowire is often characteristic of this process. The initiation of the reaction is temperature-dependent; the eutectic temperature and the temperature for silane decomposition must be reached for the reaction to proceed [10].

In practice, by applying and steadily incrementing voltage while recording the current, localized resistive heating of the suspended microbridges can be monitored. The current-voltage relationship for a representative U shaped MEMS structure is shown in Fig. 3 and additional process parameters are presented in Table 1. The current-voltage curve is characteristically linear under low input power and becomes non-linear when input power is increased, due to local high temperatures and secondary effects [16]. It is observed that the microbridge exhibited a non-linear current-voltage relation near the desired synthesis temperature. The temperature on the microstructures is characterized based on the geometry, doping level, and current-voltage characteristics [17]. Once the desired temperature range is obtained the reaction is allowed to proceed for approximately 15 minutes. At the end of the process, the gas flow is terminated and the power supplied to the microstructure is slowly decreased to prevent rapid cooling and possible thermal shock to the structures.

RESULTS AND DISCUSSION

Following synthesis, localized nanowire growth is observed. Figure 4 shows the synthesis of silicon nanowires on a 100 µm-long, 5 µm-wide polysilicon microbridge under localized joule heating for 15 minutes. The oblique view microphoto around the center region in Fig. 4(b) and the top view microphoto at the edge of the growth region in Fig. 4(c) clearly show location-dependent growth patterns as the result of non-uniform temperature distribution on the microbridge. It is believed that the microbridge in Fig. 4 has buckled towards the substrate during the synthesis process due to the compressive stress generated by the thermal expansion of the bridge structure [18]. As a result, the temperature at the center of the bridge was lowered due to better heat dissipation to the substrate, causing the nanowires, in this region to grow slower as evidenced in Fig. 4(b). Different microbridge designs are used to eliminate this effect. At the growth/non-growth interface region in Fig. 4(c), the breakdown of the thin gold-palladium film into nanoparticles is observed. However, it appears that the temperature in this area is insufficient for the formation of silicon nanowires. Relatively large sizes of the nanoparticles are formed and it is believed that the size of the nanoparticles plays an important role in nanowire synthesis; furthermore, the temperature field, the type of the catalyst and the nature of the surface could effect the formation and size of the nanoparticles.

In Figure 5 localized nanowire growth, spanning approximately 55 µm of the 100 µm long beam, originates on one polysilicon microstructure and transcends a 5 µm-wide gap to rest on an adjacent structure. The potential for these nanowires to be integrated with larger systems and serve the purpose of interconnects is clearly illustrated by this sample. The high resistivity of these intrinsic nanowires has limited their electrical analysis.

![Image](image_url)

**Figure 3.** Experimental I-V curve for sample seen in Figure 6.

**Figure 4.** Localized silicon nanowire growth on a suspended polysilicon microbridge. (a) Silicon nanowire growth spanning approximately 35 µm at the center of 100 µm long microbridge. (b) An oblique view of the nanowire growth region, showing the shorter nanowire region at the center of the structure. (c) A top view illustrating the growth/non growth interface depicting the temperature sensitivity of the synthesis mechanism.

<table>
<thead>
<tr>
<th>Device surface material</th>
<th>Device Type</th>
<th>Dimensions</th>
<th>Actuation Data</th>
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<tbody>
<tr>
<td>polysilicon</td>
<td>bridge</td>
<td>L (µm) 100</td>
<td>W (µm) 5</td>
</tr>
<tr>
<td>polysilicon</td>
<td>U shaped</td>
<td>L (µm) 100</td>
<td>W (µm) 2</td>
</tr>
<tr>
<td>SCS</td>
<td>U shaped</td>
<td>L (µm) 100</td>
<td>W (µm) 2</td>
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Table 1. Structural, geometrical and actuation data associated with the representative samples.
Figure 5. Nanowire growth localized to the central region of a polysilicon U shaped MEMS structure. The wires are seen to cross over a 5 µm gap and rest on an adjacent MEMS structure. (a) Full actuated structure shown with a parallel bridge above. (b) Closeup of nanowire growth region.

Figure 6. Nanowire growth on single crystal silicon MEMS U shaped structure.

Figure 6 shows a high-resolution SEM image of silicon nanowires on a SCS microstructure. Here the flexibility of the process is illustrated as the synthesis reaction may proceed on various MEMS platforms fabricated by different processes. In addition, the nanowire growth appears denser and individual nanowires appear straighter and stiffer in comparison to the nanowire growth in the previous two figures.

Overall, the nanowires are 30-80 nm in diameter, up to 10 µm in length and grow at rates up to 1 µm/min. The nanowire diameter is a function of the initial catalyst diameter and is seen to be larger than the catalyst [11], while the length is a function of growth time. The growth rate is believed to be related to the size of the liquid alloy as well as the synthesis temperature and gas pressure [19].

One can conclude that the localized silicon nanowire synthesis process is a strong function of local temperature, and there appears to be an “ideal temperature window” at which the reaction takes place. The gold-silicon eutectic temperature is approximately 363°C and the presence of palladium is expected to slightly increase this temperature, as evidenced in the related phase diagrams. The decomposition of silane takes place over a wide temperature range. The thermoelectric model [19] yields a characteristically parabolic temperature distribution, seen in Fig. 7 for the sample shown in Fig. 4, with hottest region located in the center of the structure. The model suggests that the reaction and therefore growth took place between 600-700°C for this sample. This model assumes sufficient doping level and a perfect crystal structure since insufficiently doped microstructures cause the current-voltage characteristic to vary considerably. This temperature estimate was confirmed with visual observation of the microstructure’s color in the nonlinear region.

As previously discussed, the resistive heating technique ideally locates the hottest region at the center of the structure. It is observed that nanowires can grow at specific regions of the microbridge depending on the profile of the applied temperature. When the ideal temperature window matches the ideal hottest region at the center of the structure, the growth region spans between 30-55% of the structure’s length. If the center temperature is too high, the majority of the growth occurs in two separated regions, relatively symmetric to the center; the extent of the growth region is decreased to only 10-20% of the total length. The smaller growth region is the result of the parabolic temperature distribution through the structure as can be observed in Fig. 7. That is, the temperature gradient is greater at points away from the center of the structure leading to more significant temperature drop over a smaller region and thereby reducing the area of the bridge spanned by the ideal temperature window. These
experimental results strongly suggest that the synthesis of silicon nanowires depends on a suitable temperature window with lower and upper limits. Since the activation of the reaction is a function of temperature, the growth is determined by the temperature regime in the microbridge. The location of the ideal temperature window for growth can be adjusted by altering the applied voltage, thus eliminating the need to lithographically define growth regions. In all growth cases, this region was stable for sufficient time to allow nanowire growth. The only limitation on this approach is the melting temperature of the microstructure (1440°C in this case for silicon). This analysis illustrates an additional advantage of this approach, as a wide temperature distribution from room to high-temperature (close to the melting temperature of silicon) can be tested to characterize the growth of nanowires at various temperatures in a single experiment.

CONCLUSIONS AND FUTURE WORK

We have demonstrated room temperature synthesis of nanowires in direct contact with MEMS structures. The process has yielded localized regions of silicon nanowires, 30-80 nm in diameter and up to 10 µm in length. Growth rates of up to 1 µm/min have been observed. Our unique process allows for immediate, direct integration of nanostructures with larger scale systems and furthermore permits the placement of these nanostructures at desired locations along the surface of the larger scale system using the concept of localized heating. This process, therefore, eliminates the need for additional assembly steps and provides a CMOS-compatible technique for the integration of nanotechnology.

Future work will focus on growth between microstructures and analysis of the electrical, thermal, and mechanical properties of the nanowires. The project’s goal is to create novel sensors based on nanostructures generated by the described technique.

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References