A MEMS Resonant Strain Sensor with 33 nano-strain Resolution in a 10 kHz Bandwidth

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Abstract—In this paper we demonstrate a high performance strain measurement system that consists of a polysilicon Double Ended Tuning Fork (DETF) resonant sensor and surface mount electronics to measure its output. This system achieves a resolution of 33 nano-strain (nε) in a bandwidth of 10 kHz, and has a noise floor of 60 pico-strain per root hertz (pε/√Hz) up to 1kHz. The 60 pε/√Hz noise floor is equivalent to a displacement resolution of 12 femto-meters per root hertz (fm/√Hz). To the best of our knowledge the smallest reported displacement resolution using surface micromachining is 16 fm/√Hz [1].

I. INTRODUCTION

Resonant sensors are an excellent choice for strain sensing because of their inherently high strain sensitivity for a given gauge length (Lg). As a result they are capable of measuring small strain fields with high accuracy [2]. The DETF sensor presented in this work has a resonant frequency of 217kHz, and Lg = 200µm. It has strain and displacement sensitivities of 39 hertz per micro-strain (µε) and 195 hertz per nano-meter (Hz/nm) respectively.

The output of the resonant sensor is frequency modulated by the input strain. Hence we require an electronic system that demodulates the signal and converts the output to digital form. In the past, phase locked-loops (PLL) have been used to perform this demodulation [3]. The output of the PLL (Fig. 1a) can then be converted to a digital signal with an analog to digital (A/D) converter. The sigma delta PLL (ΣΔPLL) shown in Fig. 1b has two advantages when compared the traditional method. First, it combines the A/D converter with the PLL. Hence it performs demodulation and digitization in one step. In addition it takes advantage of oversampling allowing simplification of the A/D converter design. Secondly, in the system shown in Fig. 1a, a voltage controlled oscillator (VCO) is used to estimate the incoming frequency. To do so the VCO is placed in the feedback loop of the PLL. Hence the output of the PLL, Vout, is a function of the scale factor, Kvco, that relates the VCO’s output frequency to its input voltage. Several parameters including temperature, and power supply affect this scale factor. As a result variation of the VCO’s characteristics (Kvco) adversely affect the resolution of the final sensor output. The ΣΔPLL uses a digital counter instead of the VCO. The counters scale factor, 1/fref, is dependent on the frequency reference, fref, used to drive it. As a result, if a high accuracy reference is used, the counters scale factor will vary much less than Kvco. Hence variation due to the VCO can be significantly reduced.

Our strain measurement system consists of a DETF oscillator described in [2] whose output is converted to a digital signal with a novel 4th order sigma delta phase lock loop (Fig. 1b). The ΣΔPLL is implemented on a PC board using surface mount circuitry and a Field Programmable Gate Array (FPGA).

II. SENSOR STRUCTURE AND OPERATION

The MEMS DETF resonant sensor was fabricated using the Robert Bosch GmbH commercial surface micromachining process [4]. The process has two polysilicon layers. The first layer is used for routing and the second is the structural layer with ~10.6 micrometer (µm) thickness. The minimum gap and beam width are 2.7 µm and 2.3 µm respectively. A photograph of the sensor is shown in Fig. 2. The DETF measured beam width is 5.67 µm and its length, which is equal to the sensors gauge length, is 200µm. Its resonant frequency, fo, was measured to be 217 kHz with a Q of 370 at atmospheric pressure [2]. An electrostatic actuator (strain actuator), shown in Fig. 2,
was used to apply an axial force and therefore an axial strain to the DETF resonator. Its purpose is for characterization of sensor. In the actual application sensors will have strain applied to the sensor through the chip substrate.

![Image](image_url)

**Fig. 2:** Photograph of DETF Strain Sensor.

### III. RESONANT STRAIN MEASUREMENT SYSTEM

The complete strain measurement system implemented in this work is shown in Fig. 3. It consists of an oscillator whose output, \( V_{\text{out}} \), is frequency modulated by the input strain \( \varepsilon(t) \). The 4th Σ∆PLL demodulates the output of the oscillator and converts it to a digital signal.

![Image](image_url)

**Fig. 3:** Resonant Sensor Measurement System.

In the past, frequency demodulation for resonant sensors has been done with traditional phase locked loops [3] (Fig. 1a). While this method is effective for some applications it has some limitations. First the voltage-controlled oscillator (VCO) is an analog block (Fig. 1a) that is used to convert input frequency into a voltage. Typically the VCO has a scale factor, \( K_{\text{vco}} \), which relates its input voltage to its output frequency \( f_{\text{vco}} = K_{\text{vco}} \times V_{\text{vco}} \). This scale factor can be a function of temperature (\( T \)), power supply voltage (\( V_s \)) etc. In addition the VCO’s output frequency is usually a nonlinear function of its input voltage i.e. \( K_{\text{vco}} \) is a function of \( V_{\text{vco}} \). For the PLL shown in Fig. 1a \( V_{\text{vco}} \) is equal to:

\[
V_{\text{vco}} \approx \frac{f_{\text{osc}}}{K_{\text{vco}}(T, V_s, V_{\text{vco}})}
\]

(1)

Where \( f_{\text{osc}} \) is the frequency of the DETF oscillator. Therefore as indicated by (1) variation in \( K_{\text{vco}} \) can degrade overall sensor performance. In addition, the phase noise of the VCO must be better than the resonant sensor oscillator to ensure the overall resolution of the measurement system is not affected by the VCO. For the VCO to have better phase noise than the DETF oscillator it would require a \( Q > 370 \). Unfortunately, high \( Q (>100) \) oscillators are difficult to implement in standard CMOS processes. The second limitation of this system (Fig. 1a) is that it would require a 13-bit analog to digital converter to meet the required 77 dB signal to noise ratio for our application (i.e. 0.1 \( \mu \varepsilon \) in \( \pm 1000 \mu \varepsilon \)).

We have chosen to use a Σ∆PLL [5] because it eliminates the disadvantages of the traditional approach. First of all, the analog VCO is replaced with a digital counter removing most of the variation and nonlinearity due to this block (Fig. 1b). We have used a crystal oscillator as a reference and hence can achieve much better phase noise and, much lower variation in the counters scale factor, \( T_{\text{ref}} = 1/f_{\text{ref}} \), than afforded by a VCO implemented on chip. In addition, unlike the VCO, the counters output period is a linear function of its input, \( N_{\text{out}} \).

Second the A/D converter is moved into the feedback loop (Fig. 1b) and is operated at \( f_s = 2 \times f_o = 434 \text{kHz} \) which is 21.7 times higher than the Nyquist rate \( f_N = 20 \text{kHz} \). Therefore the Σ∆PLL takes advantage of the inherent oversampling that exists in a resonant sensor enabling the use of a 4 bit A/D converter instead of the 13 bit A/D required by the traditional PLL implementation.

The Σ∆PLL demodulates and digitizes the input in the same step unlike the traditional system that performs this function in two steps (Fig. 1a). It does so by controlling the counters period such that its output, \( C_{\text{out}} \), is in phase with the input signal, \( V_{\text{out}} \). The loop operates by measuring the difference in time \( (e_n = t_n - \tau_n) \) between the zero crossings of \( V_{\text{out}} \) and \( C_{\text{out}} \). Then it uses \( e_n \) to estimate the length of time until the next zero crossing of \( V_{\text{out}} \) (Fig. 4). Hence \( N_{\text{out}} \times T_{\text{ref}} \) is an estimate of \( T_{\text{osc}}/2 \) where \( T_{\text{osc}} \) is the period of \( V_{\text{out}} \). The counter cannot create a signal with an arbitrary period like a VCO, but can only generate periods that are integer multiples of \( T_{\text{ref}} \). Therefore the Σ∆PLL makes a quantization error, \( q_n \), each time it estimates the sensors period. As a result, the output, \( N_{\text{out}} \), of the Σ∆PLL for a given sample is:

\[
N_{\text{out}} = \frac{T_{\text{osc}}(n)}{2 T_{\text{ref}}} + q_n
\]

(2)
The ΣΔPLL samples the period at every zero crossing, or twice the resonant frequency of the sensor. As a result the oversampling ratio, OSR = \( f_s/(2 \cdot \text{BW}) \), for this converter is 21.7.

For our application a 4th order noise transfer function (NTF) was required to meet the resolution requirements of 0.1 µε in 10 kHz. Figure 5 shows how the quantization noise is shaped (pushed to high frequency) by the 4th order ΣΔPLL noise transfer function.

This transfer function is similar to the one in [6]. It consists of two poles at DC, one from the loop filter, and one from the counter (Fig. 6). In addition, two complex poles at 10 kHz, are used to suppress quantization noise at high frequency. Finally, compensation zeros are used to ensure loop stability. Two complex zeros are implemented with the loop filter and a lead compensator is realized digitally [5] (Fig. 6).

The ΣΔPLL used in this work was implemented on a PC board using an FPGA for the control logic, counter, phase detector, and digital lead compensation (Fig. 6). In this PC board prototype the loop filter was designed with continuous-time (C-T) circuitry. Finally a 4 bit flash A/D converter was used to quantize the output of the analog filter (Fig. 6).

IV. MEASURED RESULTS

The output of a 33120A signal generator was used to measure the NTF of the ΣΔPLL. The measured NTF is shown in Fig. 7. It was observed that the measured NTF did not match the simulated NTF. Instead of having the expected slope of 40 dB per decade the measured NTF had a slope of 20 dB per decade (Fig. 7). Further experiments revealed that mismatch in the phase detector (PD) was the source of this discrepancy. The PD was implemented using standard FPGA tri-state output drivers and the mismatch in the driver’s pull-up and pull-down strength was measured to be 2 percent. Once the mismatch was incorporated into the simulation model the simulated and measured results were in good agreement (Fig. 7).
(Fig. 8). The simulation model predicted a 29 nε resolution in 10 kHz bandwidth. The actual measurement achieved a resolution of 33 nε in 10 kHz (Fig. 9). Finally, the measured noise floor is approximately 60 pc/√Hz or 12 fm/√Hz up to 1 kHz.

The measured resolution due to the resonant sensor oscillator only was 18 nε. Therefore the Σ∆PLL contributes approximately 24 nε to the overall strain measurement system resolution. Finally the measurement system was characterized by applying strain at varying frequencies to verify operation up to 10 kHz bandwidth (Fig. 10).

V. CONCLUSIONS

A complete resonant strain measurement system that obtains 33 nε in a 10 kHz bandwidth has been developed. A novel 4th order Σ∆PLL was used to demodulate and digitize the output of the resonant sensor oscillator reported in [2]. In addition this system demonstrates that using a Σ∆PLL for resonant sensing has the potential to achieve high measurement resolution, while replacing the PLL and A/D converter with one block. Thus reducing the complexity of the frequency demodulation electronics.

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REFERENCES


