VLSI MEMS Switches: Design, Fabrication, and Mechanical Logic Gate Application
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Introduction
The use of MEMS (microelectromechanical system) switches to implement digital logic was initially proposed in [1, 2]. Two important advantages of MEMS switches are their ability to survive heat and radiation. Recently, there has been increasing demand for a pass transistor replacement in specific reconfigurable computing and signal routing applications; pass transistors used in VLSI exhibit on-state resistances of thousands of ohms or more, causing signal delay and increased power consumption, particularly for FPGAs. However, traditional MEMS contact switches are typically designed and employed for RF and microwave applications and are not suitable for replacing VLSI transistors. In this paper, the design, fabrication and characterization of MEMS contact switches customized for VLSI are presented, herein referred to as “VLSI MEMS switches”. For MEMS logic and hybrid FPGA (MEMS multiplexer integrated with CMOS logic) applications, our VLSI MEMS switches have met the following specifications:

- The device size needs to be comparable to that of existing CMOS transistors.
- CMOS process compatible, no heavy metal contamination, process temperature ≤400°C.
- The contact resistance is less than 20Ω.
- The switch operates at 0μA to 100μA current level of typical VLSI transistors.

Design and Fabrication
Schematically shown in Fig. 1, a 3-terminal VLSI MEMS switch is composed of a lower Aluminum (Al) metal layer (metal 1) which is used to realize a driving electrode and a lower contact electrode. Si3N4 is employed as a dielectric layer. Finally a cantilever is made of an upper Al layer (metal 2), and when released is separated via an air gap. The cantilever is 23μm in length, 3.2μm in width, and 2000Å to 4000Å thick. The air gap is 2500Å to 4000Å. The metal1 and Si3N4 layers are 800 Å and 700Å thick, respectively. There is a contact dimple of 3μm² at the free end of the cantilever. When a DC driving voltage is applied between the lower driving electrode and the cantilever, electrostatic force pulls down the cantilever; therefore the dimple is brought into contact with the lower contact electrode. Since the switches are designed to pass 0μA to 100μA current, they are integrated with polysilicon resistors used as current-limiters or load resistors in MEMS logic gates.

The area footprint of the fabricated VLSI MEMS switches is only 0.1% to 1% of most traditional MEMS switches. Due to the fact that the cantilever length, width, and thickness are significantly less than those of traditional MEMS switches, the contact force is less than 10μN according to simulation results, compared to 100μN to 5mN contact force of traditional MEMS switches. Therefore, elimination of stiction, contact surface contamination, water vapor absorption, dielectric charging effect, and mechanical failure is challenging. To deal with these challenges, a stair-shaped electrostatic actuator (SSEA) design shown in Fig. 2 is used. Measurement results indicate that the SSEA reduces driving voltage requirement by 30%-40%. Verified by SEM (scan electron microscopy) images and destructive tests, the SSEA design also improves the robustness of the anchor sidewall, where mechanical fatigue and ultimate failures tend to occur. The switches are fabricated using a surface micromachining process illustrated in Fig. 3. An SEM image of a released switch is shown in Fig. 4.

Measurement Results and MEMS Logic Gate Application
The switches are tested using a probe station with CCD video camera and HP 4145B semiconductor parameter analyzer. The measurement results are listed in Table 1. The pull-in voltages are 10V for a 2000Å-thick cantilever and 18V for a 4000Å-thick cantilever, the release voltage of the switches is 4V to 6V. The nominal contact resistance ranges from 2Ω to 20Ω. The leakage current between the contact electrodes and between the driving electrodes are both below 1nA under 30V DC voltage. Dielectric breakdown occurs between 70V to 140V. The designed switch is utilized to build a NOT gate shown in Fig. 5 with a 980kΩ polysilicon resistor load (4.2kΩ/sq) and a 20V Vdd. The on-state current is approximately 20μA, which induces 0.4mW on-state power consumption. Simulation results suggest that, in our future research, if the sacrificial layer and cantilever thicknesses are reduced to 0.2μm and 0.1μm, respectively, the pull-in voltage can be less than 3V, and the power consumption can be reduced to less than 9μW per NOT gate.

References
Fig. 1. Cross-section schematics and design parameters of a VLSI MEMS switch connected to a polysilicon resistor.

Reduce strain level of the anchor sidewall. Driving force in this section is increased by a factor of more than 2.56.

(a) An SSEA-based switch design
(b) A traditional switch design

The traditional switch design has relatively large metal2-nitride contact area.

Fig. 2. Cross-section of a pulled-down SSEA-based VLSI MEMS switch (a) compared to a traditional switch (b).

(a) Polysilicon deposited and patterned.
(b) Al sputtered and patterned.
(c) SIN deposited and patterned.
(d) Tungsten sacrificial layer two-step patterned.
(e) Al sputtered and patterned.
(f) Sacrificial etch and critical-point dryer release.

Fig. 3. Process flow (not drawn to scale).
Fig. 4. SEM image of a VLSI MEMS switch

Fig. 5. SEM image of a NOT gate comprised of a VLSI MEMS switch and an integrated polysilicon resistor.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Measured values</th>
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<tbody>
<tr>
<td>Pull-in voltage (on voltage)</td>
<td>10V to 18V</td>
</tr>
<tr>
<td>Release voltage (off voltage)</td>
<td>4V to 6V</td>
</tr>
<tr>
<td>Nominal contact resistance</td>
<td>2Ω to 20Ω</td>
</tr>
<tr>
<td>Leakage current between the driving electrodes</td>
<td>&lt;1nA for 0V-30V bias voltage</td>
</tr>
<tr>
<td>Leakage current between the contact electrodes</td>
<td>&lt;1nA for 0V-30V bias voltage</td>
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<tr>
<td>Dielectric breakdown voltage</td>
<td>70V to 140V</td>
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<td>Resistance of polysilicon resistor load</td>
<td>980kΩ</td>
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<tr>
<td>Mechanical NOT gate on-state current</td>
<td>20 μA</td>
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<tr>
<td>Mechanical NOT gate on-state power consumption</td>
<td>0.4 mW</td>
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Table 1. List of measured results.