Annealing Nano-to-Micro Contacts for Improved Contact Resistance

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Abstract—Nano-to-micro electrical contact resistance between carbon nanotubes (CNTs) and larger-scale silicon systems are investigated using both low- and high-power annealing techniques. Carbon nanotubes locally synthesized and suspended between two silicon microbridges are used as the test platform. The annealing technique involves Joule heating of either the CNT/silicon system or the secondary silicon bridge only at low or high input power for various times. Of the 15 samples tested, results show that the contact resistance decreases for 60% of the samples and two of the 15 samples show a decrease in contact resistance greater than 50%. Higher power and longer time anneals show the greatest improvement in reducing the contact resistance. This technique can potentially reduce the contact resistance for integration of CNTs with MEMS or microelectronics systems.

Keywords—MWCNT; NEMS; MEMS; contact resistance; annealing; localized synthesis

I. INTRODUCTION

Integration of nanomaterials into larger systems for applications such as electrical interconnects or sensors is a field of intense study [1]-[3]. Nanostructures often exhibit unique properties due to high surface to volume ratios, but hindering extensive use of these materials includes placement of nanomaterials at desired locations as well as contact resistance issues when connecting them to the macroscale. As a potential solution to the first issue, we previously demonstrated that a local synthesis method based on Joule heating of the substrate allows individual or small groups of CNTs to be “placed” at certain locations on a substrate and characterized across gaps spanning 5 to 20 µm [4]-[6]. In attempts to address the second aspect of nano-to-micro integration, researchers have attempted to reduce the contact resistance by using electrical breakdown [7], silicide or carbide formation [8]-[10], electron beam irradiation [11], ultrasonic bonding [12], rapid thermal annealing [13], or Joule heating of large area Pt or Pd contacts deposited by electron beam lithography [14]-[16]. Although the methods can potentially improve the contacts, they are either expensive, heat the entire chip or device to high temperatures, require unique equipment and/or are time-consuming. Here we demonstrate a simple and fast annealing technique for locally synthesized CNTs not requiring any special or additional equipment. Preliminary results of higher temperature and longer time annealing of the secondary contact of locally grown CNTs indicates that contact resistance can be substantially reduced.

II. EXPERIMENTAL SETUP

The experimental silicon/CNT/silicon platform has been described in detail previously [4]-[6]. Briefly, two silicon microbridges are fabricated on SOI wafers with 15 µm device layers. Typically, a thin metal catalyst layer is deposited (~5nm) on the substrates using thermal evaporation or e-beam methods. The localized CNT synthesis process involves incrementally increasing the power input to one of the silicon bridges designated “growth” side, then monitoring the output voltage on the “secondary” side to determine a CNT connection. Initially, an inert gas is used to purge the chamber and growth occurs under low vacuum conditions (3.3 x 10⁻⁷ Pa). A bias voltage of up to 10 V is applied to help direct the CNT growth across the gap. A carbon source gas is flowed over the heated bridge initiating CNT growth.

After a successful CNT connection is made across the silicon microbridges, indicated by a voltage jump, multiple current-voltage (I-V) curves are then measured from -1 to 1 V with a semiconductor parameter analyzer (HP-4145B) to establish stability of the CNT and contact.
Once a stable CNT contact is verified, the annealing process is then applied. Two annealing techniques involving low- and high-temperature annealing are examined. During the annealing process, the chamber pressure is maintained at $3.3 \times 10^4$ Pa under Argon gas flowrate of 100 sccm. For low-temperature annealing, two techniques are evaluated. First, low-power annealing is applied to the entire CNT/silicon system. After CNT growth, the chamber is purged with argon gas and exposure of the sample to the ambient environment is avoided. A voltage is applied between the growth and secondary sides to generate electric current in the silicon/CNT/silicon system. Because the resistance at CNT/silicon contact is much larger than those of CNT and silicon structures, most of Joule power is consumed at the contact and the contact areas are heated locally. The voltage is then incrementally increased by 0.5 V every 5 seconds until the power of 25 to 28 $\mu$W is obtained. These lower power inputs were chosen to avoid destroying CNTs [15] as well as utilizing previous experimental evidence that higher power through the CNT system could burn-out the CNT. During the ramp-up process, three I-V measurements are taken each minute to monitor the continued stability of the CNT contact. The voltage is held constant for three minutes, then stepped down in 0.5 V increments every 5 seconds until zero voltage. Finally, initial and post-anneal I-V measurements are compared to evaluate the curve stability.

The second low power technique involves heating only the secondary bridge instead of the entire system, as shown in Fig. 1. In this case, burn-out of the CNTs can be avoided and potentially higher power values can be input into the system. The voltage of the bridge is incrementally increased 0.5 V every 5 to 10 seconds until the power input reaches approximately 30 mW, three orders of magnitude higher than the previous technique. The currents of both bridges are monitored separately. Any drastic drops in current indicate that the CNT is no longer connected to the substrate or the CNT is broken. I-V measurements are taken of the CNT/silicon system to evaluate the stability of the contact and the resulting change in resistance.

The high temperature annealing process consists of Joule heating the secondary bridge side with different power inputs. The voltage is stepped up in 0.5 V increments for 5 to 10 seconds each until the desired temperature is greater than 600 °C, which is evaluated by the emission color of the secondary bridge. The annealing processing is applied for approximately 5 minutes. The currents of both bridges are again monitored during the process to verify they are maintained steady. After annealing, multiple I-V measurements are recorded to verify that the CNT connection remains intact and the contacts are robust. Fig. 2 is a scanning electron microscopy (SEM) image of a typical silicon/CNT/silicon system. The I-V curves are used to determine the resistance of the CNT/silicon system.

To estimate the annealing temperature of the silicon bridge based on input power, we use ANSYS (version 11.0) to
TABLE I. CNT ANNEALING SAMPLES WITH PRE- AND POST-ANNEALING RESISTANCE VALUES BASED ON STABLE I-V CURVES

<table>
<thead>
<tr>
<th>CNT Sample #</th>
<th>Resistance (MΩ)</th>
<th>Metal Stack*</th>
<th>Annealing Method*</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>After growth</td>
<td>Post-anneal</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>6.8</td>
<td>3.43</td>
<td>A 3</td>
</tr>
<tr>
<td>2</td>
<td>0.25</td>
<td>0.10</td>
<td>A 3</td>
</tr>
<tr>
<td>3</td>
<td>0.54</td>
<td>0.91</td>
<td>A 3</td>
</tr>
<tr>
<td>4</td>
<td>0.12</td>
<td>0.89</td>
<td>A 3</td>
</tr>
<tr>
<td>5</td>
<td>0.11</td>
<td>0.09</td>
<td>B 2</td>
</tr>
<tr>
<td>6</td>
<td>2.1</td>
<td>1.6</td>
<td>B 1</td>
</tr>
<tr>
<td>7</td>
<td>0.54</td>
<td>0.45</td>
<td>B 2</td>
</tr>
<tr>
<td>8</td>
<td>0.07</td>
<td>0.07</td>
<td>A 2</td>
</tr>
<tr>
<td>9</td>
<td>0.46</td>
<td>0.46</td>
<td>A 1</td>
</tr>
<tr>
<td>10</td>
<td>0.45</td>
<td>0.45</td>
<td>B 1</td>
</tr>
<tr>
<td>11</td>
<td>0.23</td>
<td>0.39</td>
<td>B 1</td>
</tr>
<tr>
<td>12</td>
<td>0.053</td>
<td>0.053</td>
<td>B 1</td>
</tr>
<tr>
<td>13</td>
<td>0.098</td>
<td>0.098</td>
<td>A 1</td>
</tr>
<tr>
<td>14</td>
<td>0.16</td>
<td>0.16</td>
<td>A 2</td>
</tr>
<tr>
<td>15</td>
<td>0.42</td>
<td>0.57</td>
<td>B 1</td>
</tr>
</tbody>
</table>

* a. Metal thin films evaporated onto the bridges: (A) Fe only; (B) Mo-Al-Fe; b. Annealing methods are as follows: (1) low temperature CNT/silicon system; (2) low temperature secondary side only; (3) high temperature secondary side only

We define as change in resistance divided by as-growth resistance:

\[
\text{Resistance ratio change (\%)} = \frac{R_{\text{final}} - R_{\text{initial}}}{R_{\text{initial}}} \times 100
\]

To date, we have tested 15 samples, nine of which show a decrease in contact resistance with two samples decreasing over 50% in resistance. As shown in Fig. 5, initial and post-anneal resistance values are tabulated in histogram form. The resistance change ratios are plotted versus time and as a function of annealing temperature as shown in Fig. 6. Table 1 shows the pre- and post-annealing resistance values as well as the annealing techniques and metal layers used.

The time range for all low temperature annealing samples is three minutes or less, except for one sample that was annealed for approximately five minutes. Both low temperature annealing techniques use either the iron catalyst thin film or a multi-metal stack (Mo-Al) beneath the iron catalyst layer. Thus far no significant differences with respect to CNT/silicon resistance changes are noted at low temperatures, but will be investigated in future studies at higher power inputs and longer times. The Mo-Al stack was developed previously in our lab and has significantly improved the contact resistance between CNT forests and the substrate [17]. We use it here as an attempt to reduce the interface resistance for locally synthesized CNTs.

For higher power annealing at longer times, the secondary bridge temperature is estimated from input power values of 100 to 150 mW, corresponding to approximately 500 to 900 °C. Of the four samples annealed for longer times, all showed decreases in post-annealing resistance values with one resistance ratio decreasing over 80%.
Dong, et al., suggested that a reduction in CNT and metal electrode interface resistance is due to an increased CNT surface area in contact with the melted metal electrode material [13]. For the samples annealed at higher temperatures and longer times, this may be a contributing factor to the resistance decreases. All of those samples showed decreases in resistance ratios ranging from 20 to over 80%. While the estimated temperatures of the silicon bridges are not high enough to obtain the bulk melting temperature values of the respective metals, it has been shown that melting point depression scales with decreasing size and dimensions of the materials [18]-[19] and that the thin films on the microbridge substrates may be melting and wetting the surface of the CNT. The low temperature techniques may not be affecting the metal/CNT interface as drastically since the initial low-power annealing process through the entire CNT/silicon system involves low currents and low estimated annealing temperatures. The low temperature annealing results indicate that the contact resistance can increase or decrease under similar conditions as shown in Fig. 5. These results are in agreement with other reports in the literature [14]-[15]. In this case, the metal thin films may not be contributing to the reduction of the interface resistance by increased CNT surface area/electrode contact.

The heating of the secondary contact via secondary bridge is an effort to reduce the overall contact resistance. The resistance of the silicon bridges is on the order of several hundred $\Omega$, reported values for single MWNT resistance ranges from $\Omega$ to k$\Omega$ [20], and the electrical contact at the interface between CNTs and larger scale materials is much higher, often with values on the order of M$\Omega$. For the local synthesis silicon/CNT/silicon platform,

$$R_{\text{total}} = R_{\text{Si,growth}} + R_{\text{contact1}} + R_{\text{CNT}} + R_{\text{contact2}} + R_{\text{Si,secondary}} \tag{2}$$

where the highest expected contact resistance is at $R_{\text{contact2}}$. Thus, by heating the secondary bridge, higher temperatures can be achieved which can potentially contribute to the reduction of the overall resistance of the system by lowering $R_{\text{contact2}}$. From the higher temperature and longer time annealing sample results, trends indicate that higher power input yields improved results and will be the focus of future studies.

V. CONCLUSION

Research to improve NEMS-based contacts for large-scale integration of nanomaterials into microelectronics and microelectromechanical systems is of continued importance. Reducing the interface electrical resistance of these materials will help enable their widespread use.

Here, we have reported on fast and simple methods to reduce the contact resistance of in-situ grown CNT/silicon contacts using low- and high-temperature annealing. Two techniques were evaluated. The first involved low power inputs to the entire CNT/silicon system resulting in varied changes in resistance ratios. The second low temperature process involved heating the secondary silicon bridge only. The low power inputs again yielded varied resistance ratio results. The higher power and longer time annealing process yielded the best results with all samples showing a decrease in resistance. Overall, the experimental results indicate that annealing via Joule heating improved the contact for 60% of the samples. The high temperature samples had resistance ratio decreases from 20 to over 80%. Further work is ongoing to determine optimal temperature and time ranges for reducing the contact resistance at the NEMS interface.

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REFERENCES


