A 2.6ps_{rms}-Period-Jitter 900MHz
All-Digital Fractional-N PLL Built with Standard Cells
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Abstract — An all-digital fractional-N Phase-Locked Loop (PLL) built with standard cells and digital synthesis tools allows easier integration with digital blocks and portability to different processes or technologies. This paper presents a PLL built with standard cells and digital synthesis tools and achieves good jitter performance. It uses an embedded time-to-digital converter (TDC) with multipath to increase TDC resolution, and includes digital correction circuitry to resolve issues from clock skew. A .18µm CMOS prototype occupies 500µm x 500µm of area, generates a 900MHz clock from a 10MHz reference, has phase noise of -90dBc/Hz at 1MHz offset and 2.62ps_{rms} jitter while consuming 4.2mA from a 1.8V supply.

I. INTRODUCTION

High-performance fractional-N PLLs used in wireline and wireless communication systems require careful design by experienced and skilled analog IC designers. The design of such PLL blocks is thus expensive in terms of design time and engineering costs. In this paper, we present a PLL prototype that is built with standard cells, requires limited analog design skills, can be easily ported to different processes, and still has competitive performance.

Analog fractional PLLs and several all-digital fractional PLLs recently published use a multi-modulus divider in the feedback path to synthesize an output frequency step size that is smaller than the reference frequency [1]. This prototype uses a more digital architecture, which removes the divider and directly computes the ratio between the output and reference frequency using a counter and a TDC [2]. This ratio is then compared with a Frequency Control Word (FCW) to determine the phase difference. In this approach, phase information is converted to digital values earlier and cannot be further degraded by noise. Digital processing techniques, such as digital correction used in this prototype, can be easily incorporated into the system.

An inverter delay chain and a Vernier delay line are two simple forms of TDCs [3]. The latter can resolve resolution finer than an inverter delay, but suffers from increased area and device mismatch. In addition, calibration between the TDC and the digitally-controlled ring oscillator (DCO) is necessary in both of the aforementioned typical TDC approaches. This PLL prototype embeds the TDC within the DCO [4, 5] to achieve area reduction, require no calibration, and have good jitter performance.

II. EMBEDDED TIME-TO-DIGITAL CONVERTER

Integer-N PLLs using bang-bang phase detectors may achieve decent phase noise and jitter performance [6]. However, fractional-N PLLs usually require multi-bit TDCs as the fractional error estimators. The simplest form of TDC is a delay chain [7] as shown in Fig. 1.

Since a ring oscillator is used in this PLL prototype, as opposed to an LC oscillator, the ring oscillator is used as the TDC itself to reduce area overhead. Additionally, the delay per stage of the TDC is a fixed fraction of the oscillator period and no TDC calibration is necessary.

III. PLL ARCHITECTURE AND IMPLEMENTATION

This PLL is built entirely with standard cells, except for the custom designed current sources (shaded in yellow in Fig. 2) for ring oscillator frequency control. In addition to almost solely using standard cells, a great portion of this PLL design (shaded in green in Fig. 2) is using synthesis tools from Behavioral Verilog. Using the standard digital synthesis design flow helps realize the goal of portability to different processes or technologies with minimal effort. The circuit blocks designed using the synthesis design flow are: the binary to thermometer decoder, loop filter, arithmetic blocks, and additional digital correction circuitry.

This PLL operates as follows. The integer counter outputs the number of oscillator periods per reference period and the
phase quantizer outputs the residual fractional count of the oscillator period within each reference period. The output of the integer counter is sampled by the reference clock and multiplied by a normalization factor. This is then summed with the output of the phase quantizer, which is also sampled by the reference clock to create a feedback digital word. This feedback digital word is then compared with the frequency control word (FCW). The resulting phase difference goes through a loop filter before updating the DCO frequency.

A. Digitally-Controlled Ring Oscillator

![Fig. 3. DCO](image)

Fig. 3 shows the DCO architecture used in this prototype. Since the TDC is embedded into the DCO, the delay per stage of this DCO is directly related to the quantization noise of the TDC. To reduce the delay per stage, a DCO with multiple paths is used [8]. This reduction in delay per stage suppresses in-band phase noise introduced by TDC quantization error [7]. Their relationship follows (1).

\[
\text{PN (Phase Noise)} = 10 \log \left( \frac{(2\pi)^2 \Delta t_{\text{inv}}}{12 (2/T_O)^2 \frac{1}{f_R}} \right) \tag{1}
\]

where \(\Delta t_{\text{inv}}\) is the delay of one stage in the ring oscillator, \(T_O\) the oscillation period, and \(f_R\) the reference frequency.

![Fractional Count Diagram](image)

The DCO frequency control current source is shown in Fig. 4. There are six control bits from a binary array digital to analog converter (DAC), five bits from a unitary array DAC, and an additional five bits through a current source controlled by a 1st order sigma-delta modulator clocked at half of the DCO output frequency. The sigma-delta modulator is a five-bit accumulator whose output is the carry-out bit. The unitary array is chosen to ensure monotonicity, whereas the sigma-delta modulator is used to gain finer frequency steps in the DCO tuning [5]. Long channel devices are used in the current sources to achieve a finer frequency step, higher output impedance, greater matching between current sources, and lower flicker noise corner. The resulting DCO’s finest frequency step is 30kHz and it can operate from 400MHz to 1.3GHz.

B. Phase Quantizer

The phase quantizer is composed of an array of 26 DFFs from the standard cell library and works by sampling the intermediate nodes in the DCO. To ensure that there are no monotonicity issues due to mismatches between consecutive DFFs, a fractional count is picked when at least two adjacent DFFs outputs are high. See Fig. 5 for details. In the event that only a single DFF outputs a high, an error flag is stored. During our testing, no error flag has been detected.

![Fig. 4. Current DAC](image)

Because the pull-up and pull-down strength of DFFs may not be equal, the edge of a given stage in the DCO may be captured by the DFF before the corresponding edge of the prior stage on a given reference clock cycle. To avoid this problem, we use a differential DCO to ensure that we are always sampling the same type of edge transition. A differential DCO is chosen to achieve better TDC linearity and monotonicity. This helps reduce the magnitude of the fractional spurs in a fractional PLL.
The 26 DFFs are triggered on the rising edge of the reference clock. To avoid metastability issues, the output of these DFFs are sampled on the falling edge of the reference clock before forming the feedback digital word.

C. Loop Filter

The loop filter used in this work is a digital proportional and integral (PI) controller. The integral path ensures that the loop will not settle until the phase offset reaches zero, and the proportional path is added to help stabilize the system, as the DCO and the integral path each contribute a zero to the transfer function at DC [9]. This PI controller is shown in Fig. 6 and runs on the 10MHz reference clock. The input signal goes through the proportional path (top path in the Fig. 6) with proportional coefficient $\alpha$, and the integral path with integral coefficient $\beta$. The summation of these two paths’ outputs is the output of the PI controller. Given the bandwidth and phase margin of the PLL, the proportional and integral coefficient of the PI controller can be derived.

![Fig. 6. PI Loop Filter](image)

D. Digital Correction

Since a large portion of the PLL is designed using behavior Verilog, a digital correction scheme can be easily included in the system. An error can occur when the reference clock into the integer counter and the phase quantizer have different skews [10]. This error forces the summation of integer count and fractional count to be off by one. An example in which the reference clock arrives at the phase quantizer earlier than the integer counter is illustrated in Fig. 7. Such an error will essentially eliminate the purpose of the fractional counter. A digital correction algorithm that looks at the history of integer counter outputs is implemented to compensate for this error.

![Fig. 7. Integer Counter Error](image)

E. First Order Noise Shaping

Having the TDC embedded into the DCO results in one additional benefit. Because the quantization noise from the previous reference cycle is accumulated to the current reference cycle, there is a first order noise shaping on its quantization noise. This idea can be better illustrated with the help of Fig. 8. The total quantization noise at each reference cycle is the difference between the quantization noise from the current reference cycle and the previous reference cycle.

![Fig. 8. Noise Shaping](image)

IV. MEASUREMENT RESULTS

The prototype PLL was fabricated in a .18µm 6M1P standard CMOS process without any RF options. The design is pad-limited with an active area of 500µm x 500µm including a serial interface. The die photo is shown in Fig. 9.

![Fig. 9. Die Photo](image)

A. Phase Noise Measurement

With a 10MHz reference clock, the proportional and integral coefficient of the PI controller is set to have this PLL operate with 1MHz bandwidth and phase margin of 60 degrees. As shown in Fig. 10, the phase noise is -90dBc/Hz at 1MHz offset. The largest fractional spur is -35dBc at 400kHz offset from the center frequency. The largest reference spur is -50dBc at 10MHz offset. For comparison, Fig. 11 is the phase noise measured when the digital correction mechanism is turned off. Without the digital correction mechanism, the
integer counter mis-count disturbs the PLL from the locking states and the phase noise is degraded.

C. Comparison

Table 1 compares this work with two recently published all-digital fractional-N PLLs. Operating at 900MHz with reference clock of 10MHz, this PLL has comparable period jitter, TIE jitter and power consumption. This work occupies larger active area because our implementation was designed using a .18µm process as opposed to the 65nm processes used in [4, 5].

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TABLE I Performance Summary and Comparison

V. CONCLUSION

An all-digital fractional-N PLL built with extensive use of standard cells and digital synthesis tools is proposed and implemented. This prototype uses a differential multi-path DCO, embedded TDC, and digital correction circuitry to achieve low in-band phase noise and competitive jitter performance. Additionally, because of the widespread use of digital synthesis tools and standard cells as building blocks, this PLL has great portability to different processes and technologies.

REFERENCES