ABSTRACT

System design, component-wise fabrication and experimental thin-film evaporation results are presented for a vertically wicking micro-columnated loop heat pipe. Designed for fabrication using a three-layer wafer stack, this MEMS phase change device has components etched on both sides of the middle silicon wafer that are sealed by thinner top and bottom capping wafers. A coherent porous silicon (CPS) based dual-scale micro-columnated wick design uses a primary wick for capillary pumping and a secondary surface-micro-textured wick for thin-film liquid evaporation. For etching CPS, a Teflon based wafer-level electrochemical etching setup is implemented and results from a preliminary die-level etching study are reported. The main device components, which include the fluid transport channels, the condenser section and the columnated vapor chamber in a non-CPS base, are fabricated on silicon wafers using standard MEMS fabrication techniques. Thermal experiments are performed to study the phenomena of thin-film evaporation in a columnated open-loop micro evaporator.

NOMENCLATURE

P Pressure.
J Photocurrent.
V Voltage.
T Temperature.
k Thermal conductivity.
Q Thermal power.
A Area.

Subscripts

c Capillary.
c Cross-section.
eff Effective.
PSL Porous silicon layer.

σ Surface tension.

INTRODUCTION

The dynamics of the consumer market constantly drives new developments in the electronics industry. Moore’s law, which states that the number of transistors on a chip doubles every 18 months, is often cited in this regard [1]. The transistor size is scaled down as a result and the heat flux dissipated per unit area of the chip increases. This happens despite the fact that constant field scaling can be used to decrease power dissipation per unit transistor; Constant field scaling did not change transistor power dissipation with change in size [1]. This heat flux is further augmented by higher operating frequencies geared towards improving computation speeds. This dissipated heat has to be
removed in order to keep the electronic junction temperatures within the safe operating limit. Any thermal management solution that is employed for this purpose has to also contend with the thermal resistance of the overall electronics package if multiple chips are present. Thermal budgets for these packages have also increased considerably due to an increase in the number of chips in a multi-chip module and the number of devices in small confined spaces in systems [2]. Conventional thermal management technologies, which include metal heat spreaders at the chip level and convection air cooling at the package level, are no longer sufficient for cooling densely packaged high-thermal-budget electronic systems.

The average power density of processors with single core microarchitectures is set to reach 1000 W/cm² by the year 2015 [1]. This is within an order of magnitude of the heat flux emitted from the surface of the sun [2]. Chip designers are already limiting clock speeds and throttling device performance due to the lack of adequate cooling. Besides the consumer electronics market, the military and space sectors need high-heat-flux thermal management technologies in order to cool such devices as gallium nitride based power amplifiers, solid-state high energy lasers and space solar power generation and propulsion subsystems [2]. Several advanced cooling technologies are being currently investigated as part of a major thrust towards tackling current and future thermal management challenges facing the solid-state electronics industry. Heat pipes, loop heat pipes, microchannel heat sinks, jet-impingement, spray cooling and thermoelectric devices are among the potential contenders for high-heat-flux thermal management solutions. All of these technologies except heat pipes and loop heat pipes are active systems, which require external power for operation. A heat pipe is a passive, two-phase, high-heat-flux thermal transport system: It absorbs heat due to the latent heat of evaporation of its working fluid and transports it using the surface tension based capillary pressure generated across the liquid-vapor interface in its wicking structure. Loop heat pipes (LHP) yield improved performance over heat pipes by separating the liquid and vapor phases in the flow loop and eliminating the need for a wicking structure along the entire length of the device [3, 4]. Capillary pumped loops (CPL) are variations of loop heat pipes, where the compensation chamber is moved farther away from the evaporator section and is independently heated in order to control the operating temperature of the device.

Conventional loop heat pipes, which could carry more than a kilowatt of heat over several meters [4, 5], were bulky systems made of large cylindrical pipes. In order to enable the usage of these devices in smaller and more compact electronics, such as computers and laptops, miniaturized LHPs that can be interfaced with individual microprocessor chips have been developed [6–10]. But these devices, which feature cylindrical evaporators and transport channels made of cylindrical metal pipes, can only operate on the periphery of electronic modules. They are difficult to interface with planar electronic chips and are thus unsuited for cooling stacked electronic substrates [11], where out of plane heat dissipation is severely restricted and a thin high-conductivity substrate is required to enable the lateral dissipation of heat. Some researchers [12] have tried to develop chip-compatible LHPs, where a dual approach is undertaken: the wicking structure is microfabricated out of planar coherent porous silicon (CPS) while the compensation chamber and transport channels are kept similar to conventional LHPs. Despite a planar evaporator, these devices—although they might provide for a better interface with flat electronic substrates—still have a large size and a non-planar structure.

MEMS-based microscale loop heat pipes (mLHPs), fabricated completely on silicon and silicon carbide wafers, have been proposed in order to integrate the cooling system directly with electronic chips. These devices employ a planar wicking structure, which is fabricated by either isotropically etching channels in a Pyrex wafer [13–18] or DRIE etching rectangular channels in a silicon wafer [19, 20]. Although such an in-plane wicking structure is easy to fabricate, it exhibits limited performance since the liquid has to flow in a direction perpendicular to the incoming heat flux. This leads to non-uniform evaporation in the wick, and wick dry-out is observed at fairly low heat flux values [15]. In this paper we present the design and fabrication of a Micro-columnated Loop Heat Pipe (μLHP), which is fabricated on a silicon wafer and uses coherent porous silicon (CPS) as the base for a high-performance vertically wicking micro-columnated wicking structure. Due to its thin and planar topology, this wafer-scale ultra-high-conductivity substrate has the potential of being directly integrated into chip-scale electronics.

**MICRO-COLUMNATED LOOP HEAT PIPE**

In this section we will look at the design aspects of the micro-columnated loop heat pipe. We will first explore the structure and operation of the vertically wicking coherent porous silicon micro-columnated wicking structure. Then, we show how this wicking structure can be implemented in a silicon wafer-based loop heat pipe.

**Dual Scale Micro-columnated Wick**

The CPS based micro-columnated wicking structure has two main design features: (a) it is designed to be fabricated completely out of silicon and (b) it operates by wicking the liquid vertically onto the evaporating surface. Since there is no way to conveniently handle conventional wicking materials such as wire meshes or sintered metal powders in microfabrication processes, being able to fabricate the wick completely out of silicon is very important from the viewpoint of device integration. Also, due to the ultra-thin topology of MEMS based loop heat pipes, the planar in-plane wicking structures that have been employed until
now [13–20] are extremely inefficient and prone to failure due to wick dryout at relatively moderate heat flux values. By wicking the liquid vertically, it can be spread more evenly over the evaporating surface. This has the potential of both increasing the total amount of thin-film evaporative heat transfer and also making it more uniform over the entire heated surface.

Fig. 1 shows a 3-d design schematic of the micro-columnated wicking structure. It is a dual scale design with a coherent porous silicon primary wick, which lies in the main silicon wafer (layer 2), and a secondary wick, which straddles the top silicon capping wafer. The primary wick consists of vertical columns etched into the coherent porous silicon base. These columns interface with the secondary wick, which consists of rectangular channels etched into the top capping wafer. With its much smaller pore size, on the order of a micron or less, the primary wick can generate a large capillary pressure across the liquid vapor meniscus given by

$$\Delta P_c = \frac{2 \cos \theta}{r} \sigma$$

where \(r\) is the radius of the wick pores, \(\sigma\) is the surface tension of the liquid and \(\theta\) is the liquid-solid contact angle. As shown in Fig. 2, the main purpose of the primary wick is to use these large capillary pressures to absorb the liquid from the liquid supply side and transport it to the surface of the secondary wick for evaporation. It does this while preventing the superheated vapor from bursting through the wick into the liquid supply. Although some amount of evaporation also occurs from the liquid-vapor interface in the primary wick, most of it takes place on the evaporator surface, where the secondary wick channels are designed to maximize the overall phase change heat transfer [21].

**Device Design**

Fig. 3 shows a 3-D design schematic of the Micro-columnated loop heat pipe (\(\mu\)CLHP). The device is designed for fabrication on a three-layer wafer stack. Most of the device components will be fabricated on both sides of the middle silicon wafer (layer 2) which is about 675 \(\mu\)m thick. It will be capped on the top by a silicon wafer and on the bottom by a Pyrex wafer. The middle silicon wafer will have coherent porous silicon pre-patterned on it to serve as the base for the vertically wicking...
micro-columnated wicking structure. As shown in Fig. 3a, the columnated primary wick will face in the upward direction and interface with the secondary evaporator wick patterned on the top silicon capping wafer. The vapor and liquid transport channels and the condenser section will be etched on the bottom of the middle silicon wafer as shown in Fig. 3b. The vapor generated in the evaporator at the top will enter the vapor channel via a vapor through-hole and travel to the condenser, which is cooled by an in-built liquid-cooled heat sink patterned above it. The condensed liquid will travel via the liquid channel back to the evaporator where it will feed into the bottom of the primary CPS wick via a liquid feed-cavity. Fill ports, for degassing and filling the device with a working fluid, can be accessed via fill holes in the top capping wafer. The connecting channels from the inlet and outlet fill ports end up on the two sides of the micro-columnated wick in order to enable proper purging of the wick during a thermal-flux purging of the device to remove non-condensible gases [22].

**COHERENT POROUS SILICON ETCHING**

To start the fabrication process, we need to convert some of the silicon in the middle silicon wafer (layer 2) into coherent porous silicon (CPS). This area will have pores, going almost
Figure 5. The wafer-level electrochemical etching setup designed for the fabrication of coherent porous silicon from a plain $<100>$ silicon wafer: (a) The front of the wafer is exposed to the electrolyte in a machined Teflon container in the presence of an anodic bias and backside illumination. (b) The components of the Teflon etch container. (c) The assembled Teflon etch container with the positive and negative electrodes.

Experimental Etching Setup

Fig. 5 shows the electrochemical etching setup that we have implemented in order to obtain coherent porous silicon from a plain silicon wafer. A $<100>$ n-type silicon wafer is exposed to an electrolyte (hydrofluoric acid) inside a machined Teflon container. The wafer is clamped using a Viton O-ring with its front side in contact with the electrolyte, while its backside is exposed. The wafer is anodically biased with a voltage source, while a platinum wire dipped in the HF solution acts as the negative electrode. Current in the circuit is also measured. Backside illumination of the wafer using a lamp and appropriate optical filters is recommended as the best method for obtaining vertical cylindrical pores [23]. An ohmic contact to the silicon wafer needs to be established in order to provide a uniform potential across the wafer. When working with smaller samples, a Ga-In Eutectic can be rubbed on parts of silicon not being etched for obtaining an ohmic contact [23]. For a larger wafer, ideally, the backside of the wafer should be doped in order to create an ohmic contact. A less desirable alternative is to deposit a thin metal layer on the back, as this can potentially block the light coming from the backside illumination source. The use of 2.5 weight percent (w/o) (1.25 M/kg) hydrofluoric acid (with a few
drops of a wetting agent) as an electrolyte has been reported in literature [23]. The solution must also be stirred gently in order to remove hydrogen bubbles from the silicon surface.

Preliminary Etching Study

In order to obtain a coherent porous silicon base with accurately controlled pore diameters and trench topology, the relevant process parameters need to be properly studied and documented. Prior to processing wafer level samples in the electrochemical etching setup discussed in Fig. 5, we have conducted some preliminary die level experiments to understand the dynamics of the etching process.

Fig. 6a shows a simple die level electrochemical etching setup that was implemented without a controlled illumination source. A platinum cathode is dipped in a 25% hydrofluoric acid solution contained in a Teflon dish at room temperature. Anodic bias is applied, using an alligator clip, to the silicon die dipped in the electrolyte. Both p-type and n-type silicon samples were etched, with and without the use of pre-patterned etch pits. Fig. 6b shows that a random array of shallow pits are obtained after etching a plain p-type silicon substrate, with most of the etching happening on the surface. This result agrees with the theory of electrochemical etching, which predicts electropolishing of substrates with excess supply of holes ($h^+$). Figs. 6c-d show electrochemical etching results for a n-type silicon substrate that had pre-patterned pyramidal etch pits obtained by KOH etching. Although backside illumination was not used, some amount of trench etching was observed, with the etching taking place preferentially in the pits.

DEVICE COMPONENT FABRICATION AND TESTING

In order to realize the overall design of the micro-columnated loop heat pipe, fabrication of the main device components was undertaken. This was done in order to identify and characterize both the fabrication and performance aspects of these components. The three main processes which occur in a loop heat pipe are 1) fluid transport 2) fluid evaporation and 3) fluid condensation. While fluid transport and condensation primarily happens in channels, fluid evaporation occurs in the more complex micro-columnated evaporator.

Condenser and Fluid Transport Channels

Fig. 7 shows an array of rectangular channels that were fabricated on a silicon wafer using Deep Reactive Ion Etching (DRIE). This is a very anisotropic etching process, which cycles repetitively between etch and passivation steps to yield high aspect ratio rectangular channels with nearly vertical sidewalls. Fig. 7a illustrates the quality of channels that can be obtained; separate measurements showed that channels as small as 5 $\mu$m can be etched to a depth of 100 $\mu$m—a depth to width aspect ratio of 20 : 1.

Fig. 7b illustrates a technique used to establish a fluidic connection between larger and smaller channels without blocking some of the latter ones. A liquid meniscus in the larger channel will transition successfully to the small channels provided the distance between the channels is less than half the depth of the channels [20]. Such connections are required in the $\mu$CLHP due to the fact that some areas in the device have to be designed to be more wetting than others in order to encourage liquid occupancy in them. A similar concept is illustrated in Fig. 7c, for the channels etched inside the condenser section. The vapor condensed in this section is encouraged to drain into the liquid transport
Figure 7. Liquid and vapor fluid transport and condenser channels fabricated on a silicon wafer: (a) Parallel channels etched using DRIE. A close up view showing the near-vertical sidewalls of the channels (inset) (b) Fluidic connections between larger and smaller channels (c) Monotonic channel cross-sections designed to avoid fluid entrapment due to capillary effects in channels.

channels by virtue of a decreasing channel cross-section in that direction.

Columnated Vapor Chamber

A standalone columnated vapor chamber was designed and fabricated in order to study and quantify thin-film evaporative heat transfer inside the proposed micro-columnated wicking structure. Fig. 8a gives an overview of the design and mechanism of operation of this test structure. Hollow columnar structures, inside a rectangular cavity, are etched into the bottom silicon wafer (floor) in order to simulate the fluid supply function of the primary CPS part of the micro-columnated wick. The top silicon wafer (ceiling) is micro-textured with either parallel or criss crossing $2 - 16 \mu m$ wide channels. The wafers are diced and the two components are reversibly bonded together using a packaging assembly.

Liquid thin-film evaporation in the vapor chamber is implemented as follows: Liquid is supplied to the columns of the vapor chamber by a syringe-pump-fed cavity interfaced with the bottom of the device. Heat flux is applied at the left end of the ceiling; it travels laterally and reaches the micro-textured surface, where it results in the evaporation of the incoming liquid. The vapor formed in the chamber exits through the parallel channels, which are etched into the floor leading from the chamber to the end of the device. Figs. 8 b & c show a number of different floor and ceiling samples that were fabricated for inclusion into the vapor chamber test structure. The spacing between the columns in the floor design can be varied to study its effect on the rate of evaporative heat transfer, due to the effect it has on the distribution of the liquid-vapor meniscus. Similarly, a number of different micro-texture patterns can be tested to determine the
topologies that maximize evaporation.

**Experimental Study of Thin-film Evaporation**

Fig. 9a shows an Infrared (IR) image of the open-loop micro-evaporator setup that was used for studying the phenomena of thin-film evaporation inside the columnated vapor chamber. As discussed in the previous section, a known heat flux is applied to one end of the ceiling of the vapor chamber using a ceramic heater. The chamber is supplied with liquid from a fixed-flow-rate syringe pump. As the heat flux travels along the length of the device, some of it is absorbed by the liquid, while the rest travels to the other end of the device, where an ice-cooled metal block acts as a constant temperature heat sink.

The temperature profile on the surface of the device is measured with an IR camera, to obtain a measure of the amount of heat flux that goes towards thin-film evaporation in the columnated vapor chamber; Average cross-section temperatures at two points along the length of the device are used to calculate the temperature gradient $\Delta T / \Delta x$ on the surface of the evaporator. The in-plane effective thermal conductivity of the device is then given by

$$k_{\text{eff}} = \frac{Q}{A_c} \frac{\Delta x}{\Delta T}$$

where $Q$ is the ceramic heater power input and $A_c$ is the area of cross-section of the device. The above model is verified by measuring $k_{\text{eff}}$ for the case where there is no water in the device. The measured value is found to be close to the actual value of thermal conductivity for silicon, which is approximately 100 W/mK at a temperature of 100°C.

Now, it can be theoretically derived that the evaporative heat flux exhibits a non-linear proportionality to the measured value of $k_{\text{eff}}$. This effective thermal conductivity is plotted in Fig. 9b vs time as the heater is turned on, after the liquid flow rate to the device and the heater voltage have been fixed. Due to the onset of evaporation in the vapor chamber (at $t \sim 32$ s), $k_{\text{eff}}$ rises to a value of almost 2000 W/mK from an initial theoretical value of 100 W/mK (for pure silicon). This result qualitatively demonstrates the large evaporative heat fluxes that are associated with thin-film evaporation in a columnated-wick vapor chamber topology. A similar behavior can therefore be predicted for the proposed CPS-based micro-columnated wicking structure, with the capillary pumping in the CPS pores supplying the working fluid instead of the syringe pump.

**CONCLUSIONS**

Design and fabrication aspects of a wafer-based micro-columnated loop heat pipe were presented. The device is designed for fabrication using a three-wafer stack, with the components etched on both sides of the middle silicon wafer and capped by top and bottom wafers. The structure and operation of the dual-scale micro-columnated wicking structure was discussed, and the complementary roles of the primary and secondary wicks were outlined. An experimental setup was designed and implemented to define a coherent porous silicon base on a silicon wafer, by performing illuminated electrochemical etching in hydrofluoric acid. Preliminary electrochemical etching results, from experiments performed on die level substrates, agree with the predictions of the theoretical model governing electrochemical trench etching in silicon. The main µCLHP device components were fabricated using MEMS patterning and etching techniques. Thin-film evaporation in a columnated open-loop micro-evaporator was experimentally studied to verify the...
expected phase-change behavior of the CPS columnated-wick design.

Acknowledgments


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