ABSTRACT
A simple yet versatile, lithography-free process has been demonstrated to make direct-write, self-aligned graphene Field Effect Transistors (FETs). The critical step to define the source, drain and the top-gate electrodes is achieved by the near-field electrospinning process and the electrospun polymer fiber is utilized as the gate dielectric material. Fabricated FETs show a carrier mobility at 5056 cm²/Vs which corresponds to a typical graphene carrier density of n=10¹² cm⁻². Three distinctive advancements have been achieved as compared with the state-of-art technologies: (1) top-gate graphene FETs utilizing a lithography-free process; (2) polymer fiber as the top-gate oxide material; and (3) dual functions/operations as top-gate or back-gate FETs. As such, the proposed self-aligned, direct-write graphene fabrication process could open up a new class of manufacturing path for graphene-based microelectronics.

KEYWORDS
Graphene, Electrospinning, Field Effect Transistor (FET), Lithography-free, Nanofiber

INTRODUCTION
In recent years, graphene-based field effect transistors (GFET) have been reported to achieve devices with high cut-off frequency, [1] high on-off ratio [2] for applications in amplifiers and RF mixer [3,4]. However, most of these previous works used conventional or e-beam lithography processes to define the graphene transistors. These rather complex processes could cause extra spaces between the gate and source/drain regions, resulting in additional channel resistance [5]. Furthermore, the deposition of the inorganic gate dielectrics often requires surface functionalization with high temperature treatments, leading to undesired damages of graphene lattice [6]. Here we propose a self-aligned, direct-write graphene transistor fabrication process to alleviate these challenges by directly writing organic gate dielectrics on graphene and patterning source/drain and gate electrodes by way of self-alignment.

Figure 1a illustrates the conceptual schematic diagram of the device utilizing Near-Field Electrospinning (NFES) [7] as the key process feature. Isolation trenches are constructed for the separation of devices and NFES is followed to deposit polymer fiber as shown. A blank metal deposition is used to define the contact pads. The cross-sectional view of the FET region in Figure 1b shows that the electrospun fiber not only separates the top gate and channel and acts as the gate dielectrics, but also defines top gate and source/drain electrodes in the self-aligned manner. Thanks to the cylindrical shape of the fiber, the metal layer on top of the fiber will not be in contact with the source and drain electrode. The metal on top of the fiber is connected to the “top electrode contact” as marked in Figure 1a by using silver paste as shown. The whole back substrate can be used as the back electrode.

Figure 1: a) Conceptual illustration of the direct-write GFET. The top gate (TG), source (S) and drain (D) electrodes are self-aligned as defined by the electrospun fiber and the follow-up metal deposition process. b) Cross-sectional view of the device showing LGR (local graphene region). The electrospun polymer fiber serves as both gate dielectrics and the self-aligned mask to define the source and drain regions during the metal deposition process. The GL area is minimized as the theoretical channel length is the same as the diameter of the fiber.

FABRICATION
The device fabrication process is illustrated in Figure 2. A 285nm-thick silicon dioxide layer was thermally grown on a p-type silicon wafer and a single layer graphene (grown separately using CVD method) was transferred onto the substrate [8]. The quality of the single layer graphene is verified using Raman spectroscopy [9]. The device/contact areas were patterned (Figure 2a) and etched in oxygen plasma (50 Watts for 5 seconds) to remove graphene...
A dry-etched process (350 Watts for 1 mins in C4F8 plasma) was followed to remove the oxide layer (Figure 2c). An isotropic, timed XeF2 etching process was then used to remove part of the silicon to create undercuts of about 1 μm (Figure 2d). This process provided good isolations between electrodes. In the prototype devices, a polyvinylidene fluoride (PVDF 20 wt%) fiber of 0.8 μm in diameter was electrospun under a voltage of 0.8 kV (Figure 2e). A blank metal deposition was followed with 2 nm-thick chrome/10 nm-thick gold layer by e-beam evaporation (Figure 2f). Silver paste was then applied to the top-gate for electrical connection.

Figure 2: Fabrication process flow.

Figure 3a shows the top view optical photo of the device after the near-field electrospinning process. Five possible electrode areas can be identified in this figure, including S (source), D (drain), TG#1 (top gate #1), TG#2 (top gate #2) and BG (back gate). The width of the graphene channel has also been defined in this process and two different widths, 10 μm for SAMPLE #1 and 100 μm for SAMPLE #2, have been designed in the prototype devices. The length of the channel is the same as the diameter of the fiber which is 800 nm for the prototype devices. The timed isotropic silicon dry etching can create an undercut beneath the silicon dioxide layer. As such, some portions of the oxide film at the etching edges will be suspended after the etching process. Due to the possible residual stress effect, the suspended oxide layer has resulted in some natural curvature/optical effect as shown in Figure 3b. This undercut is designed to prevent electrical connection between the silicon substrate (back gate) and the contact electrodes after the blank metal deposition process.

Figure 3: (a) Optical image of SAMPLE #1 after the near-field electrospinning process showing the five contact pad regions, including source (S), drain (D), top gates (TG#1 and TG#2) and back gate (BG). The electrospun fiber goes from TG#1 to TG#2 and in-between the source and drain electrodes. (b) A close up view optical photo at the region between the source and drain areas showing the curvature of suspended silicon dioxide due to residual stress. The scale bars are 10 μm in both photos.

A good adhesion force between the polymer fibers and graphene substrate helped the fiber to stick to the substrate. However, after the gold deposition process, the adhesion force became weaker but the silver paste at both ends of the fiber seemed to provide good mechanical supports during the experiments without any fiber rotation or movement. Figure 4a shows the SEM image of the electrospun fiber lying across the contact pads from the SAMPLE #2 and the isolation trenches separating the individual electrode regions can be clearly observed. A close up SEM image is shown in Figure 4b where the trench has a design width of 4 μm. The trench distance is designed to be as small as possible such that the mechanical strength of the polymer fiber can support itself to go across the gap. It is found that the gap distance can be as large as 10 μm without affecting
the rigidity of the polymer fiber to across the trench. The image shows clearly that the electrospun fiber has successfully defined the source and drain regions for a self-aligned graphene channel transistor. Furthermore, the suspended oxide/graphene layer close to the trench area has shown some slight curvature which is also observed in the optical photo in Figure 3b. The metal layer on top of the graphene area seems to be smooth while it is a bit rough on top of the polymer fiber.

Figure 4: (a) SEM image of SAMPLE #2, scale bar 10 µm, and (b) a zoom in view on the trench region, scale bar 1µm. The diameter of the fiber is around 800 nm.

RESULTS AND DISCUSSION

Experimentally, the $I_{DS}-V_{DS}$ curve under different back gate voltage is measured and shown in Figure 5a. The top gate is grounded through the measurement as shown in the inset. The linear response of each branch indicate a quasi-constant graphene channel resistance under each back gate voltage and ohmic contact between the gold electrode and graphene layer under $V_{DS}<0.1$V. No obvious channel current saturation is observed under $V_{DS}$ as high as 1V. The slope of the curve reaches the local minimum when $V_{BG}=-2$V and shows a carrier mobility of 5056 cm²/Vs given a typical carrier density of $n=10^{12}$ cm⁻² at the Dirac Point. Figure 5b illustrates the $I_{DS}-V_{GATE}$ transport characteristics of both top gate and back gate. As expected, the $I_{DS}-V_{GATE}$ responses show the ambipolar symmetric behavior and reach the minimum current at the Dirac Point. Three regions (I, II, III) can be identified according to the Dirac Points of the two characteristic curves. As the $|V_{GATE}-V_{Dirac}|$ increases, the electron concentration in the region I of top gate and region I, II of back gate increases, as well as the holes concentration in the region II, III of top gate and region I of back gate, resulting a V-shape trace. Compared to the back gate, the top gate has a smaller channel current at the Dirac Points. This could be the result of different LGR (local graphene region) between the dual gate operations. During the back gate operation, the whole distance between source and drain can be considered as active LGR. For the top gate operation, the effective LGR could be smaller than the default value of LGR as illustrated in Figure 1b due to circular geometric effects. This could lead the LGR of top gate to be smaller than that of the back gate as suggested by the experimental results in Figure 5b.

The total carrier density inside the graphene channel can be approximated by [10]:

$$n_{total} = \sqrt{n_0^2 + n[V_{GATE}]^2}$$ (1)

where $n[V_{GATE}]$ is the gate induced channel carrier density and $n_0$ is the residual impurities which lead to a non-zero channel current at the Dirac Point. The gate induced carrier density can be further expressed by $n[V_{GATE}]=C_{GATE}(V_{GATE}-V_{Dirac})$, where $C_{total}$ is the total gate capacitance. The inset in Figure 5b indicates the serial relationship between $C_{TG}$ (top gate dielectric capacitance), $C_q$ (graphene channel quantum capacitance) and $C_{BG}$ (back gate dielectric capacitance) during the operation. The gate capacitance equals to the serial of gate dielectric capacitance and a quantum capacitance which is ignored here for simplicity.

Figure 5: (a) $I_{DS}-V_{DS}$ measurement of SAMPLE #2 and the top gate is grounded throughout the measurement as shown in the inset. (b) $I_{DS}-V_{GATE}$ measurements of SAMPLE #1 under dual gate control. The inset indicates the serial relationship between $C_{TG}$ (top gate dielectric capacitance), $C_q$ (graphene channel quantum capacitance) and $C_{BG}$ (back gate dielectric capacitance) during the operation.
The horizontal shift of Dirac Point is observed in Figure 5b. This is because the residual impurities from the air could have doped the graphene as n-type [11], thus a negative gate voltage is required to neutralize the residual carrier $Q_{res}$ to reach the Dirac Point. As $Q_{res}=C_{GATE}V_{GATE}$, a ratio of $C_{TG}/C_{BG}$ will result in a similar ratio of $V_{DRAC,BG}/V_{DRAC,TG}$. As shown in Figure 6, the COMSOL simulation of the top gate dielectric capacitance gives the electrical potential distribution between the semi-cylindrical gold terminal and grounded graphene channel. An electrical potential of 1V is applied on the gold shell and a terminal charge of $-6.79 \times 10^{-16}$ C is calculated from the simulation results under $\varepsilon_r \approx 1$ for air and $\varepsilon_r \approx 7.9$ for PVDF. The calculated effective $C_{TG}$ is $8.48 \times 10^{-9}$ F/cm$^2$. The back gate capacitance, $C_{BG}$ can be calculated as $\varepsilon_r \varepsilon_0/d_{SiO2}$, where $d_{SiO2}$ is the thickness of the oxide layer. If one uses $\varepsilon_r = 3.9$ for SiO$_2$, $C_{BG}$ is calculates as $1.21 \times 10^{-8}$ F/cm$^2$ and the ratio of $C_{TG}/C_{BG}$ is 0.70 which corresponds well to the ratio of $V_{DRAC,BG}/V_{DRAC,TG}$, which is 0.66 in this case.

CONCLUSION

Direct-write polymer fibers to construct self-aligned top gate graphene channel FET has been successfully demonstrated. The near-field electrospinning method was used to generate arbitrary pattern of PVDF fibers as the mask and the polymer fiber was used as the gate dielectrics for graphene channel FETs. Both conductance ($I_{DS}/V_{DS}$) and transconductance ($I_{DS}/V_{GATE}$) of the graphene FET have been measured with a carrier mobility of 5056 cm$^2$/Vs has been derived. Both vertical and horizontal shifts of the Dirac Points have been observed from the top and back gate operation results, and this could be the results of different LGR and different effective gate dielectric capacitance, respectively. In summary, a lithography-free process has been successfully developed to fabricate graphene FETs with submicron channel length as well as self-aligned source/drain regions. This simple, fast, and effective process provides new opportunities for further mass production of graphene based electronics.

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REFERENCES


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