An accurate, low-power, and highly integrated solution for accurate assessment of body fat is presented that addresses a growing consumer interest in economical and easy-to-use solutions for monitoring personal health and fitness. Unlike the prevalent present solution that estimates body fat percentage from an impedance measurement integrated in a weight scale and gives only a global index with accuracy compromised by a host of factors including skin moisture and metabolic activity, the reported approach uses ultrasound for an accurate measure of the actual thickness of the fat and muscle layers [1].

The ASIC has 7 identical channels each with 6b delay control with 5ns resolution for transmit beam-forming, high-voltage level shifters, and a receive/transmit switch that isolates the low-noise receiver from the high transmit voltage. Unlike previously published solutions [3] that rely on external high-voltage supplies, this design generates all the necessary voltage levels from a single 1.8V supply with on-chip 5V and 32V charge-pumps and is thus amenable to battery power or power from a smartphone.

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Figure 11.8.1 shows a block diagram system comprising an ASIC and custom MEMS transducer. The latter consists of an array of AlN piezoelectric micromachined ultrasonic transducer (PMUT) array with 50μm diameter, 70μm spacing, 8MHz resonant frequency and Q=3 [2]. In the experiments reported here, the array is organized into 7 groups of 9x5 elements where each group is wired in parallel and actuated with 32V square-wave drive signals generated by the ASIC, which results in a 3mm peak membrane displacement. The total capacitance C, of each group is 17.5pF and dominated by pad and wiring parasitics.

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Figure 11.8.2 shows the dynamic 32V level-shifter. The conventional solution exceeds the current capabilities of on-chip charge-pumps owing to the large crowbar current flowing during the switching transient. The dynamic shifter adds switches Msw+ and Msw- to prevent a conducting path from the supply to ground. Msw+ is opened before the low-to-high transition of Vin and closed after the output has settled. This effectively removes the pull-up Msw+ from the output during the transition, thus enabling the use of a small NMOS pull-down Mn+ with low input capacitance and permitting high-speed operation.

Switches Msw+, and Mn+ are high voltage transistors and thus require high-voltage controls themselves. This requirement is met with an auxiliary level-shifter. The primary and auxiliary shifters, Cells A and B in Fig. 11.8.2, are cross-coupled to generate all required control signal, as indicated in the timing diagram. The input to Cell B is delayed by τ = 10ns with respect to the input control of Cell A. During reception, the transmitter is inactive. Charge leaking from Vr+ could eventually turn on Mn+ resulting in crowbar current. Inactivity of more than 10ms turns on a bypass switch that ensures Vr+ remains at HV0. Since a small device can be used, the circuit has minimal impact on operating speed and power dissipation. An identical circuit is used for Vr-.

Figure 11.8.3 shows the block diagram system comprising an ASIC and custom MEMS transducer. The latter consists of an array of AlN piezoelectric micromachined ultrasonic transducer (PMUT) array with 50μm diameter, 70μm spacing, 8MHz resonant frequency and Q=3 [2]. In the experiments reported here, the array is organized into 7 groups of 9x5 elements where each group is wired in parallel and actuated with 32V square-wave drive signals generated by the ASIC, which results in a 3mm peak membrane displacement. The total capacitance C, of each group is 17.5pF and dominated by pad and wiring parasitics.

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Figure 11.8.4 shows the startup waveform of the dynamic level-shifter. A 10μs and consumes 2.6μJ from the 1.8V supply. Thanks to the dynamic level-shifter, power loss within level-shifter is negligible and 89% of energy from the charge pump is delivered to drive the output transducers. The charge pump delivers 32.5% of the power from the 1.8V supply to the 32V charge pump output and hence dominates overall system efficiency. In this work, the transmitter is driven at 8MHz, although the level-shifter is capable of operation up to 40MHz. 28ns latency is measured from input pulse to output. 17.5pF.

Figure 11.8.7 shows the micrograph of the AlN transducer array and the ASIC fabricated in 0.18μm CMOS with 5V and 32V high-voltage transistors and 5V VMOS capacitors. The chip area is 2.0mm2 and includes the complete system except for the digital controller, ADCs, and two off-chip storage capacitors.

References:
Figure 11.8.1: System diagram comprising the ASIC, ultrasonic transducer, and a controller realized with an FPGA.

Figure 11.8.2: Conventional static and proposed dynamic 1.8V to 32V level-shifter design with crow-bar current suppression for low-power operation.

Figure 11.8.3: Circuit diagram of the charge-pumps and clock generators. The same design is used for the 5V and 32V pumps.

Figure 11.8.4: Measured charge-pump startup transient. The graphs show the tradeoff between ripple and startup time versus bypass capacitor size and efficiency and available power versus clock speed.

Figure 11.8.5: Received echo and 2D reconstructed image from a tissue phantom [5].

Figure 11.8.6: Performance summary and measured thickness of fat layer versus phantom.
Figure 11.8.7: Die photo for AlN transducer array and ASIC.