Wafer-Scale Silicon Photonic Switches beyond Die Size Limit

TAE JOON SEOK 1,2,3, KYUNGMOK KWON, 2,3, JOHANNES HENRIKSSON, 2, JIANHENG LUO, 2 AND MING C. WU 2,3*,

1School of Electrical Engineering and Computer Science, Gwangju Institute of Science and Technology, Gwangju 61005, South Korea
2Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, Berkeley, CA 94720, USA
3These authors contributed equally.
*wu@eecs.berkeley.edu

Abstract: Fast optical switches have been proposed as a promising alternative to enable continual scaling of data centers with increasing size and data rates. Silicon photonics is a compelling platform for large-scale integrated photonic switches, leveraging the advanced manufacturing foundries for electronic integrated circuits. In the past decade, the port counts of silicon photonic switches have increased steadily to 128x128. Further scaling of the switch is constrained by the maximum reticle size (2–3 cm) of lithography tools. Here, we propose to use wafer-scale integration to overcome the die size limit. As a proof of concept demonstration, we fabricated a 240x240 switch by lithographically stitching 3x3 array of identical 80x80 switch blocks across reticle boundaries. Stitching loss is substantially reduced (0.004 dB) by tapering the waveguide width to 10 μm. The fabricated switch on a 4 cm x 4 cm chip exhibits a maximum on-chip loss of 9.8 dB, an ON/OFF ratio of 70 dB, and switching times less than 400 ns. To our knowledge, this is the largest integrated photonic switches ever reported. The loss-to-port count ratio (0.04 dB/port) is also the lowest.

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1. Introduction

Silicon photonics is a disruptive technology for large-scale photonic integrated circuits (PIC) [1], thanks to its ability to use complementary metal-oxide-semiconductor (CMOS)-like fabrication resulting in high-volume production at low cost. In addition to optical transceivers for datacom and telecom, silicon photonics also made inroads into a wide variety of applications such as programmable photonics processors [2,3], photonic neural network circuits [4], optical phased arrays [5,6], and integrated photonic switches [7]. Many of these applications benefit from integrating a large number of photonic elements, leveraging the high integration density and uniform, high-yield process of silicon photonics.

Large-scale photonic switches have attracted much attention for applications in data center networks [8–12]. Several research groups have reported large-scale silicon photonic switches [7,13–18]. Two of the reported switches have port count ≥ 32x32 and on-chip loss ≤ 6 dB [7,18]. Further scaling of the switches faces two challenges: (1) high optical loss and (2) maximum chip area limited by the reticle size of lithography. To overcome the cumulative loss in Mach-Zehnder interferometer (MZI) and microring resonator (MRR)-based multi-stage switches, we have proposed a new micro-electro-mechanical-system (MEMS) switching mechanism that has nearly zero loss in the BAR state [7]. Using a crossbar architecture, all but one switching elements are in the BAR state. Thus, large switches with low loss can be realized. We have successfully demonstrated a 128x128 switch [19] on a 1.6x1.7-cm² die, which is approaching the maximum size allowed in a single reticle (usually around 2 to 3 cm for typical deep-UV lithography steppers or scanners). Wafer-scale integration have been
employed to create long delay lines across multiple reticles [20]. However, each reticle requires a distinctive mask.

In this paper, we present wafer-scale integrated silicon photonic switches that overcome the reticle size limit. Identical switch blocks are stitched lithographically with loss < 0.004 dB. As a proof of concept, we experimentally demonstrated a 240x240 switch on a 4x4-cm$^2$ die by stitching a 3x3 array of 80x80 switch blocks. The maximum on-chip loss of the longest optical path is measured to be 9.8 dB. This is the largest integrated photonic switch ever reported in any integrated photonic switches. The loss-to-port count ratio of 0.04 dB is also the lowest.

Fig. 1. (a) Schematic of ultra-large-scale silicon photonic switches. The switch consists of the three basic building blocks: 1) an NxN switch, an Nx1 input coupler, and a 1xN output coupler. (b) Schematic of the NxN switch block. The waveguides are tapered to a wider width to reduce stitching loss. (c) Unit cell of the silicon photonic MEMS switch consisting of a pair of adiabatic couplers on orthogonal bus waveguides with MMI crossing.

2. Ultra-large-scale switch architecture

Figure 1 shows the schematic of the ultra-large-scale silicon photonic switch architecture. The switches consist of three basic building blocks: 1) an Nx1 input coupler block, 2) a 1xN output coupler block, and 3) an NxN switch block. Each block fits within a single reticle of a step-and-repeat lithography stepper (or scanner). The input coupler couples light from N input
fibers to N silicon waveguides. These waveguides are connected to the western ports of the switch array. Similarly, the output coupler block is attached to the southern edge of the switch array and couples light to N output fibers. Either grating or edge couplers can be used for the coupler blocks. The NxN switch block is based on matrix architecture with N input, N through, N add, and N drop ports at western, eastern, northern, and southern edges, respectively. By stitching MxM array of the switch blocks during lithography, an NMxNM switch is realized. M input coupler blocks and M output coupler blocks are also stitched to western and southern sides of the switch array to provide NM input/output coupler ports. The waveguides are tapered to a wider width to reduce the scattering loss at reticle boundaries, as shown in Fig. 1(b). Switch fabrics with different sizes can be realized by simply varying number of the switch blocks without changing mask reticles. Multiple switch fabrics with different sizes can be integrated on a single wafer. In our experimental demonstration below, M = 3, N = 80, and MN = 240.

The MEMS switching element is similar to what we reported previously [7]. It consists of orthogonal bus waveguides with multimode interference (MMI) crossing on the first layer and a pair of vertically-actuated adiabatic couplers on the second layer [Fig. 1(c)]. The multilayer adiabatic coupler switch with MEMS actuation offers many advantages: (1) zero loss in the OFF (BAR) state as the coupler is far from the bus waveguides; (2) low propagation loss using wide ridge waveguides with shallow etch, and (3) extremely high extinction ratio (> 60 dB) and low crosstalk (< -60 dB) over a broad wavelength range (> 100 nm). The cumulative loss commonly seen in other silicon photonic switches are completely eliminated. This is a key factor to achieve ultra-large-scale switches with low loss. The detailed designs of MMI crossings and adiabatic couplers can be found in [7].

Fig. 2. Numerical simulation of the scattering loss caused by 100-nm misalignment at the stitching interface. The inset shows the schematic of the simulated structure. Silicon rib waveguides are designed to have 220 nm thickness and 60 nm partial etch depth.

The offset between adjacent reticles in our deep-UV stepper (ASML 5500/300) is less than 100 nm. Though small, it can cause significant stitching loss in sub-micron waveguides. The misalignment loss can be drastically reduced by widening the waveguides at the joints. Figure 2 shows the simulated misalignment loss of stitched silicon rib waveguide with a thickness of 220 nm, an etch depth of 60 nm, and a misalignment of 100 nm. For silicon waveguide with 1 μm width, the loss is larger than 0.1 dB. The stitching loss reduces to below 0.004 dB as the waveguide width increases to 10 μm, the designed tapered width of our waveguide.

3. Experimental result
The ultra-large-scale silicon photonic switches were fabricated using the 6-inch wafer processing facilities in Marvell Nanofabrication Laboratory at UC Berkeley. All three building blocks (input, output, and switch) have a footprint of 1 cm x 1 cm [Fig. 3(a)]. Each switch block consist of 80x80 silicon photonic MEMS switches whose unit cell has a footprint of 110 μm x 110 μm [Fig. 3(b)]. We have successfully realized a 240x240 silicon photonic switch by arranging a 3x3 array of the 80x80 switch blocks and attaching the input and output coupler blocks at the western and southern edges of the switch array, as shown in Fig. 3(a). To ensure the continuity of stitched waveguides, adjacent blocks were exposed with 5-μm overlap. The widths of the stitched waveguides are tapered to 10 μm to reduce the stitching loss as discussed in the previous section. Figure 3(c) shows the microscope image of the stitched waveguides. The nominal offset between adjacent blocks is measured to be about 70 nm from the close-up scanning electron micrograph (SEM) in the inset of Fig. 3(c). The full arrangement of the switch and coupler blocks on the SOI wafer is described in Supplement 1.

Fig. 3. (a) Fabricated 240x240 silicon photonic switch on a 4 cm x 4 cm die. (b) Optical micrograph of the unit cell in silicon photonic MEMS switch. Unit cell size: 110 μm x 110 μm. (c) Tapered waveguides at the stitching interface. Inset: close-up SEM image of the waveguide edge 70 nm offset at waveguide joint. (d), (e) Perspective view SEM images of fabricated silicon photonic MEMS switches.
To characterize the switch, a custom measurement setup was built with two motorized 6-axis stages to align the two fiber arrays with the input and output coupler blocks. Two 80-channel fiber arrays with 13-degree polishing angles are used to interface with the switch. With this setup, we can probe any 80x80 switch blocks by moving the fiber arrays along the input or output couplers. As the ultra-large-scale switch can be readily extended to wafer-scale device, the stages were designed to have 10-cm translation range. The experimental setup along with the fabricated switch are shown in Fig. 4. TE polarized-light is coupled in and out of the switch through grating coupler arrays. The coupling loss was measured to be ~4.5 dB/facet at 1500 nm wavelength. The switch was electrically addressed using a pair of probe tips.

![Image of experimental setup with 240x240 silicon photonic switch]

Fig. 4. Experimental setup with the 240x240 silicon photonic switch.

![Graphs showing measured switching characteristics and spectrum]

Fig. 5. (a) Measured switching characteristics showing digital switching behavior with an extremely high extinction ratio of 70 dB. (b) Measured switching spectrum confirming broadband operation.
Figure 5(a) shows the switching characteristics of a typical switch cell. When the bias voltage increases, the adiabatic couplers on the upper layer are pulled down to the bottom layer at 40 V, directing light from input bus to the output bus waveguides. The switch stays in the ON state with further increase in voltage as the coupling distance is precisely defined by microfabricated mechanical stoppers. The switch turns off when the bias voltage decreases below 25 V. This digital switching characteristics without requiring precise bias controls is a key advantage of silicon photonic MEMS switches. These features are particularly beneficial for large-scale switch fabrics with a large number of actuators (57,600 in this switch). The MEMS switch exhibits an extremely high ON/OFF (extinction) ratio of 70 dB, which results in exceptionally low crosstalk. In the OFF state, the switch has no loss, effectively eliminating the loss accumulation in large switch matrices. The broadband spectral response due to the adiabatic couplers is observed [Fig. 5(b)], which makes the switch compatible with WDM (wavelength division multiplexed) signals. The temporal response is shown in Fig. 6. The ON and OFF switching times were measured to be 400 ns and 300 ns, respectively, for a 65-V square-wave voltage waveform. The ON switching time can be shortened by increasing the bias voltage though the OFF switching time is limited by the stiffness of the MEMS springs. Shorter switching time and lower bias voltage are possible by further optimization of the MEMS actuators.

To characterize the on-chip loss, we measured two hundred randomly selected switch configurations. The measured on-chip loss vs the number of switching cells in the light path is plotted in Fig. 7. From the linear fitting, the loss-per-cell and the switching loss are extracted to be 0.019 dB/cell and 0.7 dB, respectively. The maximum loss of the longest optical path is 9.8 dB (= 0.019 x 478 + 0.7). The switching loss of 0.7 dB is likely due to the high propagation loss in polycrystalline waveguides and adiabatic couplers. It is expected that optimization of the polycrystalline silicon deposition condition can significantly reduce the switching loss [21]. The propagation loss and the crossing loss in crystalline silicon bus waveguides are main causes of the loss-per-cell. We measured these passive losses from test structures on the same wafer. The waveguide propagation loss and the crossing loss were characterized to be 0.45 dB/cm and 0.016 dB/crossing, respectively (see Supplement 1). This results in a loss of 0.019 dB/cell (= 0.45 dB/cm x 70 μm + 0.016 dB), which agrees well with the experimental data in Fig. 7.
4. Conclusion

We have demonstrated wafer-scale 240x240 silicon photonic switches on 4x4 cm² dies by stitching 3x3 array of 80x80 photonic MEMS switch blocks, 3 input coupler blocks, and 3 output coupler blocks. The width of bus waveguides is tapered to 10 μm at the stitching locations, resulting in negligible stitching loss as low as 0.004 dB. The switch exhibits a maximum on-chip loss of 9.8 dB, an ON/OFF ratio of 70 dB, and switching times less than 400 ns. To our best knowledge, these are the largest integrated photonic switch and the lowest on-chip loss (0.04 dB/port) ever reported.

The proposed switch architecture overcomes the die size limit by the reticles. Reducing the optical loss is another critical factor for further scaling of photonic switches. For an example, the longest optical path of a 1000x1000 switch would have 1999 crossings in the current matrix architecture, which results in a loss of 32 dB from the crossings alone, assuming the same crossing loss of 0.016 dB. One possible solution to eliminate waveguide crossings is to use multilayer bus waveguides as reported in [22,23]. The crossing loss, which contributes about 80% of loss-per-cell in the current architecture, will be reduced down to a negligible level, leaving the propagation loss as the main source of the loss. Moreover, the unit cell footprint can be further reduced (by about 30%) without the MMI crossing, resulting in higher integration density and lower loss. Waveguides made in state-of-the-art silicon photonics foundries have propagation losses of 0.1~0.2 dB/cm (shallow-etched silicon rib waveguides). It is projected that 1000x1000 switch with ~ 1.5 dB (~ 0.1 dB/cm x 75 μm/cell x 2000 cells) on-chip loss is achievable.

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