Poly-SiGe MEMS for Modular Post-CMOS Integrated Microsystems

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Outline

• Introduction
  - Motivation for modular integration
  - Alternative integration approaches

• Poly-SiGe as a MEMS material system
  - Basic material properties
  - Process integration
  - Demonstration platform: RF MEMS

• Conclusion

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Example: MEMS Gyroscope

A. Seshia et al., IEEE MEMS 2002 (Las Vegas, Nevada)

Resonant mass: 700 \( \mu m \times 700 \mu m \times 2 \mu m \), suspended 2 \( \mu m \) above substrate

Structural material: poly-Si

Why not build the gyroscope on top of CMOS?
CMOS/MEMS 1.02 MHz Oscillator

- Pierce sustaining amplifier co-fabricated in Sandia 2 μm CMOS-last iMEMS process

300 nm-thick poly-Si interconnect: low-pass filter!

DETF resonator with drive and sense electrodes

200 μm

Why Modular Integration?

✓ Allows for separate development and optimization of electronics & MEMS processes

- **MEMS first:**
  - Electronics and MEMS cannot be stacked
  - IC foundries are wary of pre-processed wafers

- **MEMS last:**
  - Chip area can be minimized
  - IC foundry can be used, if MEMS thermal budget is low

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DMD™ Projection Display Chip

- Several added layers of metal (Al and alloys)
  - photoresist sacrificial material

Each mirror corresponds to a single pixel, programmed by an underlying SRAM cell to deflect light either into a projection lens or a light absorber.
CMOS Post-Processing

- Composite structural layer:
  - poly-Si and metallization layers
    → electrical connections
  - single-crystal Si
    → better mechanical properties

- CMOS process + 3 etches:
  1. backside Si etch
  2. frontside dielectric etch
  3. frontside Si etch (release)

- Advantages:
  ✓ no add-on materials needed
  ✓ low parasitic capacitance
MEMS in the Metallization Stack

J. L. Lund et al., 2002 Solid-State Sensor, Actuator and Microsystems Workshop

Composite structural layer:
- thin metal layer → electrical connection
- thick dielectric layer → good mechanical properties

Fixed beam resonator (vertically actuated)

✓ Can stack MEMS directly on top of (Bi-)CMOS
  → low parasitic resistance and capacitance, small chip size
The Ideal MEMS Technology

For low cost and high performance, we want:

- **Low thermal process budget**
  - can use semiconductor foundry for electronics

- **Capabilities similar to poly-Si MEMS**
  - can leverage MEMS foundry processes
  - can leverage MEMS industry design experience
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Why SiGe?

- SiGe can be processed at significantly lower process temperatures than Si ($\leq 450^\circ$C)
- Conventional process tools can be used
  - LPCVD & RIE
- Properties are similar to those of Si, and can be tailored by adjusting Ge content
- Significant IC industry experience
  - heterojunction BJTs, MOS gate electrodes, strained Si substrate
Tystar20 LPCVD Poly-SiGe MEMS Reactor
UC Berkeley Microfabrication Laboratory

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Carrie W. Low, BSAC
Ge as a Sacrificial Material

- Ge-rich films etch rapidly in oxidizing solutions
  - non-HF-based etchant (heated H₂O₂)
    → eliminates need for protective layer for electronics
  - high etch selectivity to poly-Si, SiO₂, Si₃N₄, metals

### Etch Rates (µm/min)

<table>
<thead>
<tr>
<th>Material</th>
<th>HF</th>
<th>RCA, SC1</th>
<th>H₂O₂*</th>
<th>Cl₂/HBr Plasma</th>
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</thead>
<tbody>
<tr>
<td>Poly-Ge</td>
<td>~0</td>
<td>3.0</td>
<td>0.4</td>
<td>0.41</td>
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<tr>
<td>Poly-Si₀.₂Ge₀.₈</td>
<td>~0</td>
<td>0.75</td>
<td>0.08</td>
<td>0.37</td>
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<td>Poly-Si₀.₄Ge₀.₆</td>
<td>~0</td>
<td>0.06</td>
<td>~0</td>
<td>0.31</td>
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<tr>
<td>Poly-Si</td>
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<td>~0</td>
<td>~0</td>
<td>0.16</td>
</tr>
<tr>
<td>Annealed PSG</td>
<td>3.6</td>
<td>~0</td>
<td>~0</td>
<td>~0</td>
</tr>
</tbody>
</table>

*J. M. Heck et al., Tranducers’ 99*
SiGe-MEMS/CMOS Technology

A. E. Franke et al., Solid-State Sensor and Actuator Workshop Technical Digest, pp. 18-21, June 2000

- Conventional CMOS process (Al metallization)
- Structural layer: ~65% Ge, 2.5 μm thick deposited by LPCVD at 450°C (1 μm/hr), in-situ B doped (6 Ω/□)
- Sacrificial layer: 100% Ge, 2 μm thick deposited by LPCVD at 450°C (~1 μm/hr)
Integrated SiGe-MEMS/CMOS

Resonator next to Amplifier
- conventional layout

Resonator on top of Amplifier
- smaller area --> lower cost
- reduced interconnect parasitics
  --> improved performance


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Si$_{0.35}$Ge$_{0.65}$ Resonator Response

19.6kHz comb-drive: Q ~ 31,100

S. A. Bhave et al., *Solid-State Sensor and Actuator Workshop Technical Digest*, pp. 34-37, 2002
Properties of P+ poly-Si$_{0.35}$Ge$_{0.65}$ as deposited at 450$^\circ$C

- $E = 155 \pm 5$ GPa
- Stress = -10 MPa (compressive)
- Stress gradient $\approx 10^{-4}/\mu$m for a 2-$\mu$m-thick film
  - 100 $\mu$m cantilever beam bends up 0.7 $\mu$m at the tip
- Fracture strain = 1.2 $\pm$ 0.1%
  - comparable to poly-Si
- $Q = 31,000$ at 20 kHz in vacuum
Optimized Deposition Process

Poly-Si$_{0.4}$Ge$_{0.6}$ as deposited at 450$^\circ$C

Pressure: 600 mTorr
Dep. rate: 0.6 $\mu$m/hr
Residual stress: -9 MPa
Strain gradient: $2.4 \times 10^{-5} \mu m^{-1}$
(2 $\mu$m film)

Deflection of 1 mm beam: 12 $\mu$m

This process is now available through the MEMS Exchange

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(http://www.mems-exchange.org/)
Effect of Lower $T_{deposition}$

Poly-$\text{Si}_{0.4}\text{Ge}_{0.6}$ as deposited at $425^\circ\text{C}$

Pressure: 600 mTorr
Dep. rate: 0.5 $\mu\text{m}/\text{hr}$

Residual stress: $-45$ MPa
Strain gradient: $3 \times 10^{-4}$ $\mu\text{m}^{-1}$

Deflection of 1mm beam: 150 $\mu\text{m}$
Low Thermal-Budget Techniques

- Pulsed ELA modifies the microstructure near the surface → can be used to tune stress and stress gradient:

- Shallow absorption depth (~20 nm) + short pulse (~40 ns) → negligible thermal exposure of underlying films

S. Sedky et al., 2002 MRS Fall Meeting, Paper J4.2

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Motivating Application: Poly-SiGe Integrated RF MEMS

Poly-SiGe RF MEMS technology

Shielded Interconnect to Drive Electrode

DC Bias to Resonator

5-level metal foundry CMOS

Microshell Encapsulation (anchors not shown)

Drive Electrode

RES

Sense Electrode

Shielded Vertical Signal Path to Gate of Input Transistor

R. T. Howe, T.-J. King, and A. P. Pisano, DARPA MTO NMASP Projects.
Poly-SiGe Technology for RF Resonators

- Planar bulk-mode acoustic modes
- Maximize capacitive transduction efficiency → high aspect ratio nanogaps (50 to 100 nm)

- Spacer technology challenges:
  - Selectivity of $\text{H}_2\text{O}_2$ sacrificial etch
  - Step coverage

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Brian Bircumshaw *et al*, IEEE MEMS '04
Simpler Poly-SiGe Resonator Process

- Damascene on Ge-Blade Process Sequence

Damascene on Poly-Ge Blade Process

- Blade definition by resist ashing
- High Aspect Ratio (17:1) Germanium Blade etching
- SiGe structural layer deposition
- Cross section of a released DETF
VHF Poly-SiGe Resonator Measurements

Bulk Longitudinal Resonator

RF/LO Technique

74 MHz Fundamental Mode

205 MHz Third Harmonic

F_m = 74.4 MHz
Q = 2863
V_p = 40V
Pressure = 2mT
P_RF = 10dBm
V_LO = 10Vp-p at 10MHz
Output Gain Stage = 20dB

F_m = 205.35 MHz
Q = 3540
V_p = 40V
Pressure = 4mT
P_RF = 25dBm
V_LO = 10Vp-p at 10MHz
Output Gain Stage = 20dB

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Emmanuel Quévy, et al, Hilton Head 2004
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Conclusions

• Integration of MEMS with foundry electronics can lead to enhanced functionality and/or performance
  → Range of applications will expand in the future

• Different approaches are possible
  The best choice will likely depend on the application

• Low-temperature (<450°C) poly-SiGe can leverage MEMS foundry processes & design infrastructure
  Work is in progress to demonstrate poly-SiGe RF MEMS technology with integration on sub-micron CMOS
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