Industrial Challenges for MEMS Manufacturing

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Bio Info

- BSAC 2001 – 2006
  - Advisors: Prof. Roger Howe, Prof. Tsu-Jae King Liu
  - Ph.D. Thesis *Novel Processes for Modular Integration of Silicon-Germanium MEMS with CMOS Electronics*
- Silicon Clocks / Silicon Labs 2006 – 2015
  - Monolithically integrated CMOS and MEMS using poly-SiGe
- Intermolecular 2015 – 2017
  - ALD / PVD equipment and materials study
- InSense 2017 - 2019
  - Monolithically integrated CMOS and MEMS using specialized Cu as the mechanical material.
- TDK InvenSense 2019 – present
  - Wafer-to-wafer bonding for direct integration of MEMS and CMOS

- All of my jobs have 

connections.

Lab to Fab

Microlab / Nanolab

Goal – Graduation
- Have one working device to publish a few papers.
- New users do not break the equipment before the paper's deadline.

Process engineer's job
- Long hours in the cleanroom
- Do everything

SILICON CLOCKS

Startup

Goal – IPO / change the world
- Demo the technology with one working device.
- The product has a market.
- Foundry partner willing to bring the process to mass production.

Process engineer's job
- In cleanroom once a while
- Prepare instruction for operator
- Set up special tool, recipes

TDK InvenSense

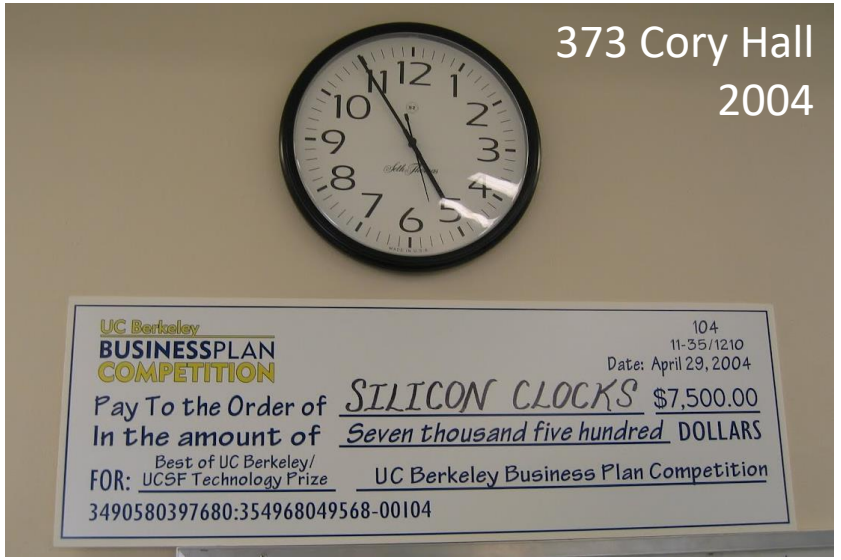
Major MEMS Company

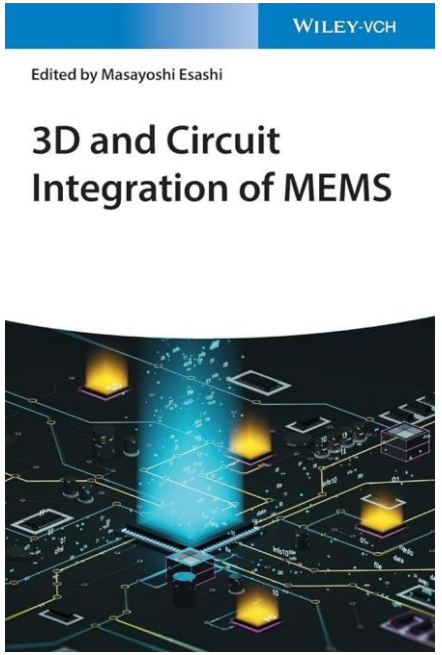
Goal – Commercial success
- Ship millions of parts
- Product meets customer spec
- Cost control at foundry
- Consistency in yield and quality

Process engineer's job
- Not allowed in the cleanroom
- Communication with internal teams and foundry partner

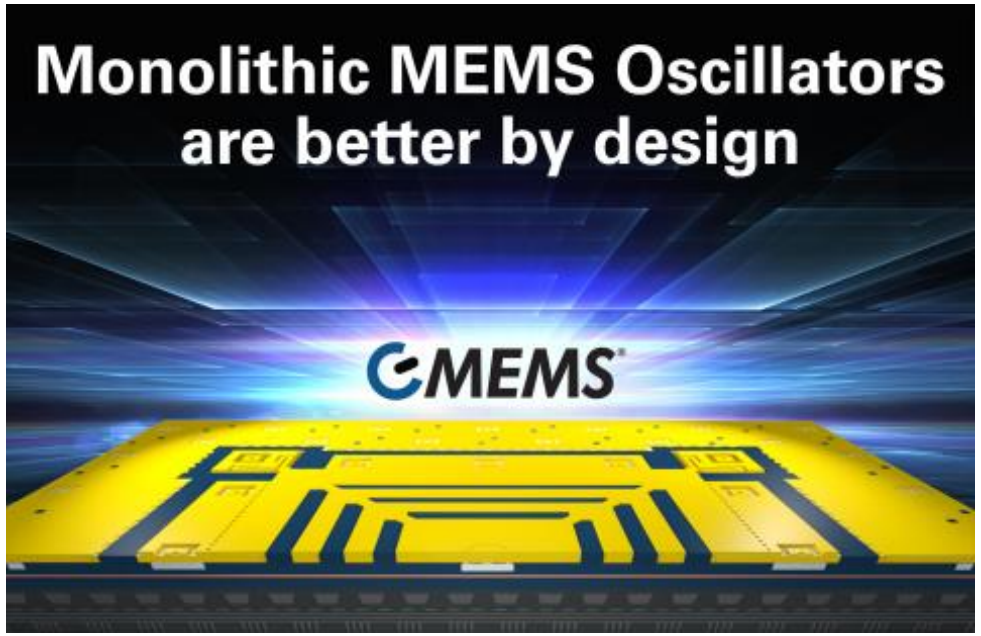
CMEMS® History

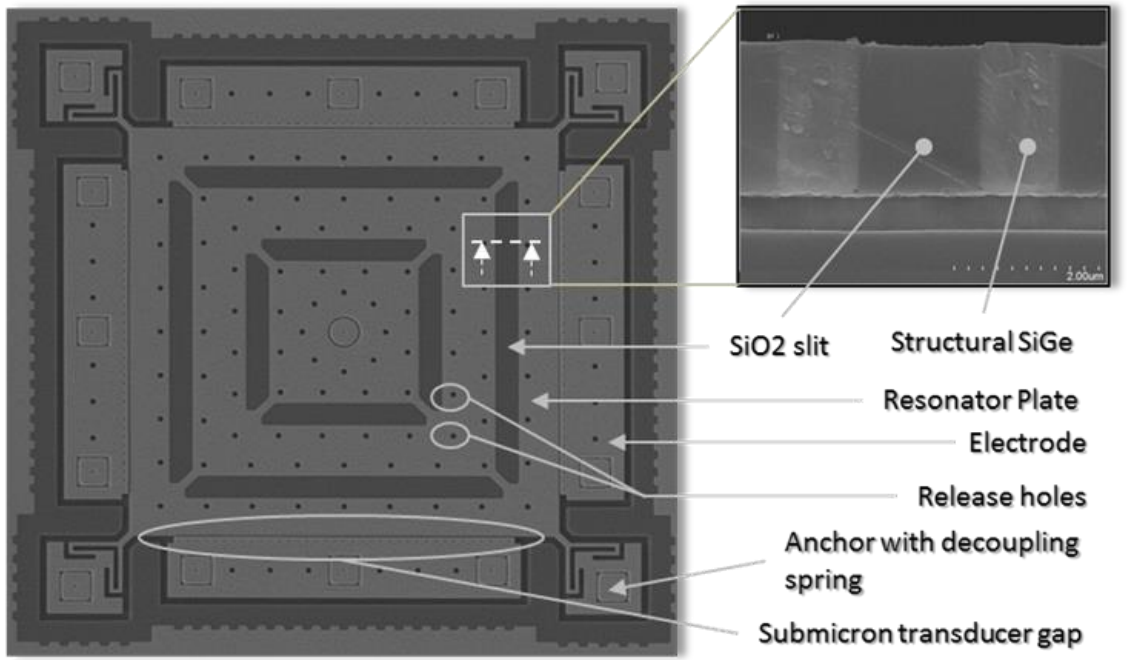
- ~2000 – SiGe MEMS research led by Roger Howe and Tsu-Jae King Liu at Berkeley
- 2004 – Business plan competition at Haas School of Business
- 2006 – Silicon Clocks founded
  - MEMS resonator to replace quartz crystal as timing reference
  - Make SiGe a standard process platform in the foundry, like a CMOS process
- 2010 – Silicon Clocks acquired by Silicon Labs
- 2013 - CMEMS® Resonator announced
- 2015 – Silicon Labs changed strategic direction and CMEMS® became history
- 2021 – "Poly-SiGe Surface Micromachining", Chapter 5 in *3D and Circuit Integration of MEMS,* M. Esashi, Editor (Wiley-VCH, Germany), 2021





CMEMS ® Resonator



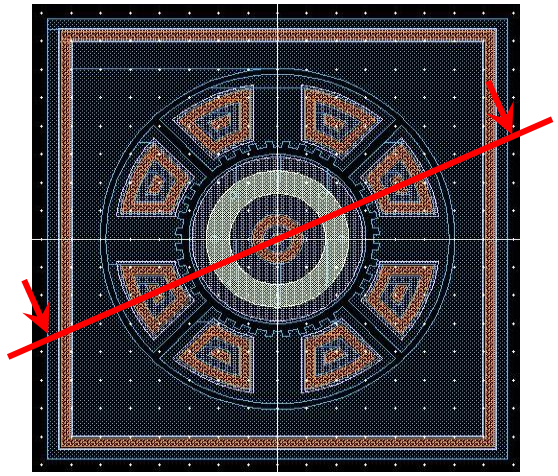


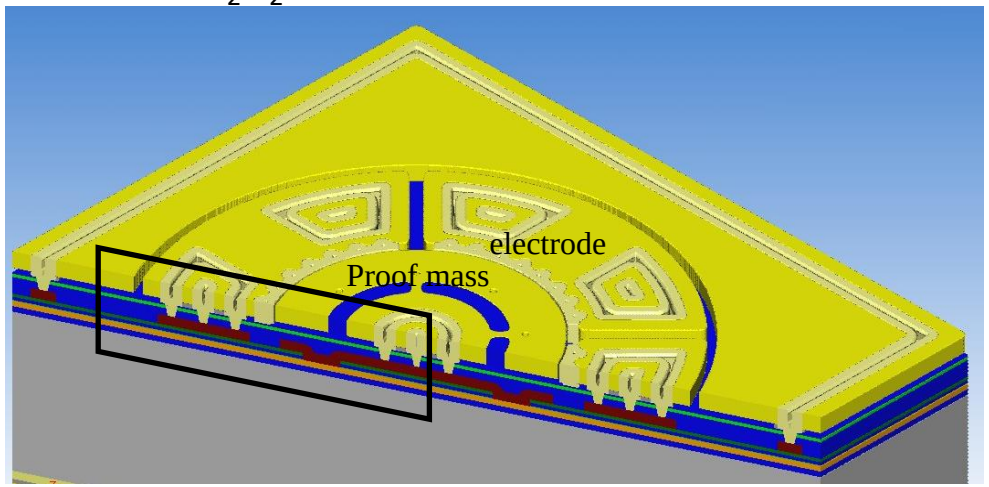
E. P. Quévy, "CMEMS® Technology: Leveraging High-Volume CMEMS Manufacturing for MEMS-Based Frequency Control", a white paper published by Silicon Laboratories, June 2013

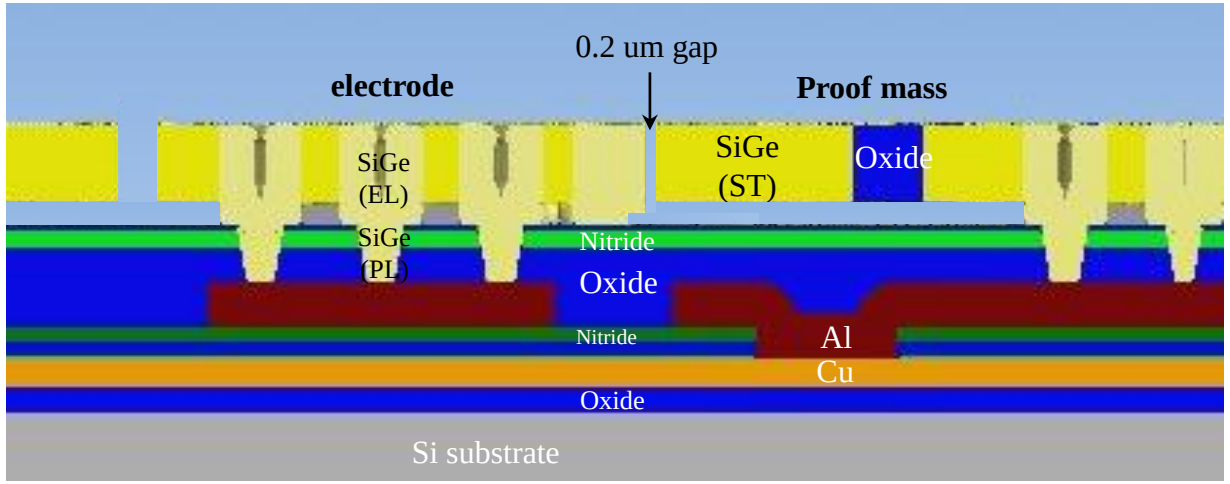
- SiGe MEMS resonator built directly on top of standard CMOS wafer
- Oxide-filled slit for temperature compensation
  - SiGe gets softer as temperature increases
  - Oxide gets harder to compensate the temperature drift
- 0.2 µm electrostatic transducer gap
- 0.5 µm line feature-size

CMEMS® Process – CMOS + MEMS

- 6 masks surface micromachining process
- Starting material – 0.13 µm CMOS wafer, with Al as top metal
- SiGe via as electrical connection to CMOS
- Poly-SiGe structural material
  - CMOS compatible process temp
  - Similar mechanical properties as poly-Si
- Oxide slit embedded in proof mass for temp compensation
- Ge sacrificial layer
- 0.2 µm gap defined by Ge spacer
- Heated H_2O_2 release

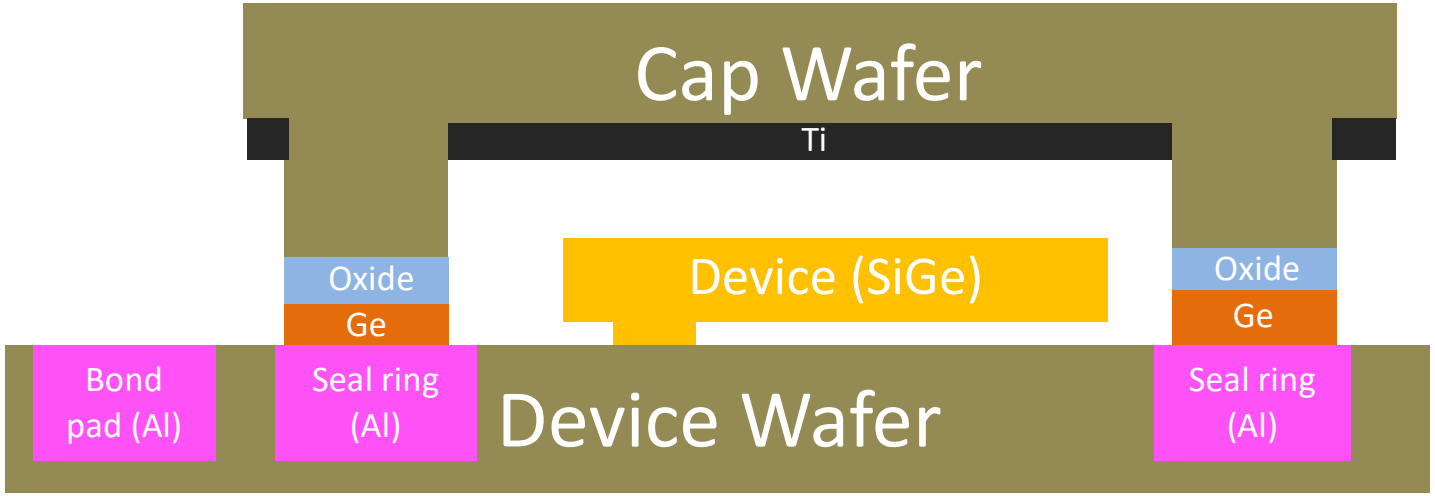






E. P. Quévy, "IC-compatible MEMS structure", U. S. Patent 7,514,760, Apr 7, 2009
E. P. Quévy, C. W. Low, J. R. Hui, Z. Gu, "Technique for Forming a MEMS Device", U. S. Patent 8,852,984 B1, Oct 7, 2014

CMEMS® Process - Encapsulation



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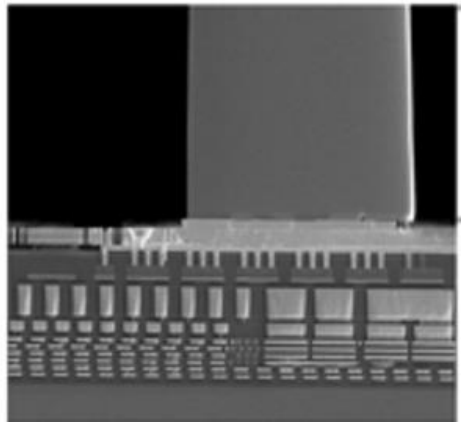

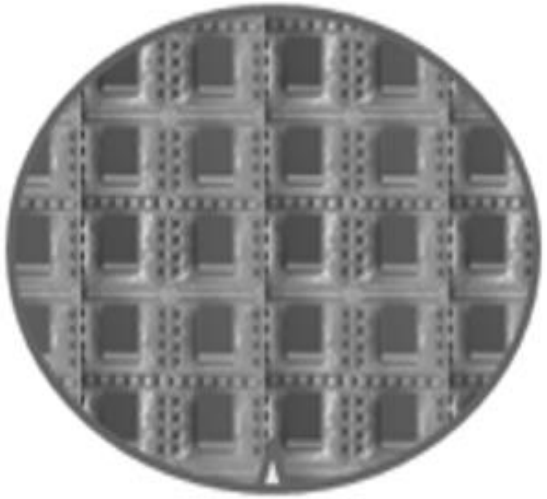

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- Al-Ge eutectic bonding
  - CMOS wafer's top metal Al serves as bond pad and eutectic bonding seal ring
  - Ti getter for pressure stabilization
- Grinding
- Half dicing to expose bond pad for wafer level electrical test

CMEMS® Process Development

SILICON CLOCKS SILICON LABS

- Initial research done at Microlab
  - Limited daytime equipment availability
- 1st working device built at SVTC (Silicon Valley Technology Center)
  - Set up run card for operators to run non-critical steps
  - Module development done by Si Clocks engineers
    - Heavy use of wafer level SEM inspection tool for decision making
  - Detailed documentation to prepare for fab transfer
- Process bring-up at SMIC (Semiconductor Manufacturing International Corporation)
  - Documented step-by-step process description with SEM images
  - 3 Si Labs engineers took turns to stay in SMIC for ~3 years.
  - > 95 % yield

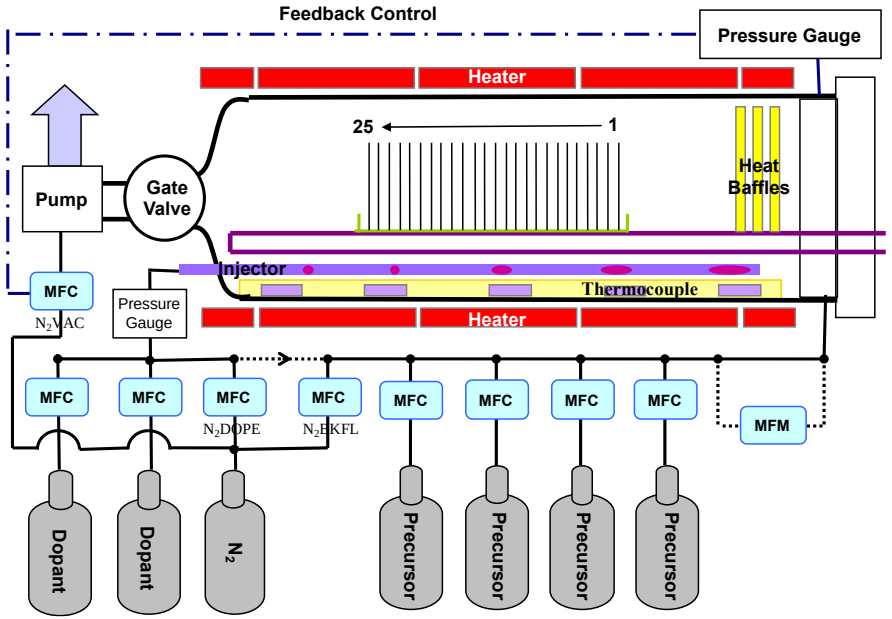
CMEMS®

CMEMS® Manufacturing Challenges

- Most of the process steps and equipment were standard at SMIC, except SiGe process
- Business discussion
  - Startup vs. big foundry
  - Capital expense for the SiGe furnace
  - Resonator would be a good business after mass production
  - Bigger picture – SMIC could become the MEMS foundry with the SiGe process so that design houses can be their future customers
- Technical discussion
  - Manufacturability
  - Throughput
  - Cost analysis

Poly-SiGe Furnace Lab to Fab

- 1st generation SiGe furnace (Tystar) at UC Berkeley for R&D
  - Materials properties study
  - Focused on maintenance friendly (BCl_3 development, MFM monitoring)
- 2nd generation SiGe furnace (Aviza) at SVTC
  - Focused on repeatability and uniformity
  - Lessons learned in particle control
- 3rd generation SiGe furnace (Hitachi KE) at SMIC Chengdu & Shanghai for production
  - Focused on throughput, uniformity, SPC control and maintenance friendly



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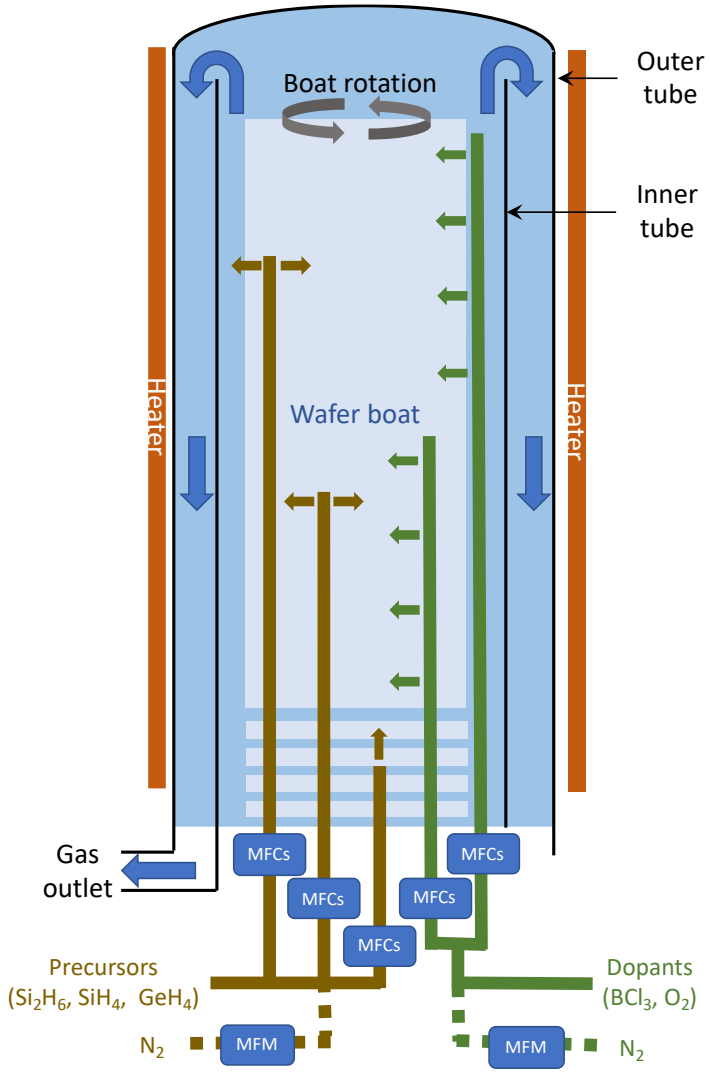

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Why didn't CMEMS® technology mature to market?

SILICON CLOCKS SILICON LABS

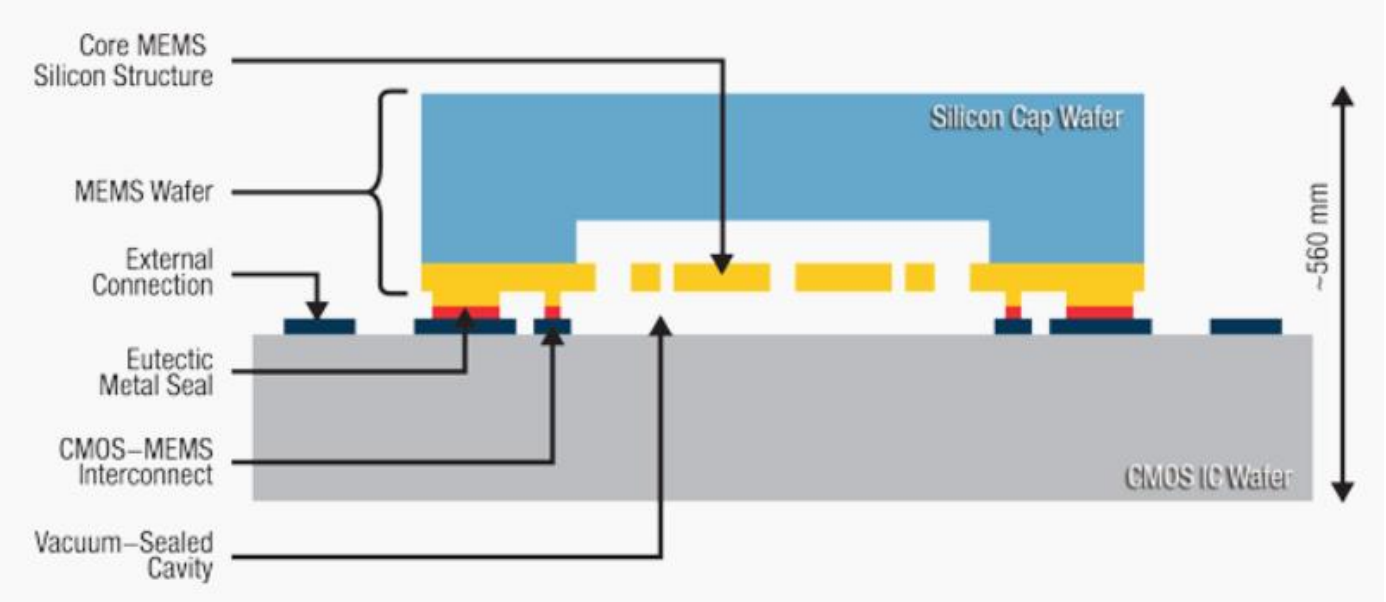
- Quartz crystal got cheaper, and the projected MEMS resonator market got smaller
  - Some design issues were discovered at late stage
  - ~ 1 year wasted to move from SMIC Chengdu to SMIC Shanghai
  - Team distracted to work on inertial sensors for some time
- When Silicon Labs decided to change direction from MEMS, some VCs and SMIC were interested in funding the CMEMS® technology as a late-stage startup.
  - SLAB kept all the CMEMS® related patents.
  - A few years later, SLAB sold the CMEMS® related patents to SMIC.

CMEMS®

TDK InvenSense Overview

- InvenSense founded in 2003; BSAC alum Joe Seeger was one of the co-founders
- IPO in 2011
- Acquired by TDK in 2016
- Successful model of MEMS design house with outsourced fabrication
- MEMS Sensors
  - SmartMotion™ (Accel and gyro)
  - SmartSonic™ (Ultrasonic Time-of-Flight sensors)
  - SmartSound™ (Microphone)
  - SmartPressure™ (Pressure sensor)

Nasiri-Fabrication Process (Motion Sensors)



https://invensense.tdk.com/technology/

- Wafer-to-wafer bonding for direct integration of MEMS with standard CMOS wafer
- Cost effective process and compatible with high volume foundries
  - Use commercially available equipment
  - Standard off-the-shelf processes
  - Single crystal Si structural material
  - Wafer-level hermetic sealing and electrical interconnect

Nasiri-Fabrication Process – Si Cap

https://invensense.tdk.com/technology/

- Silicon cap wafer
  - Etch to define the inertial sensor cavity volume

Nasiri-Fabrication Process – Core MEMS

https://invensense.tdk.com/technology/

- Core MEMS wafer
  - Single crystal silicon as MEMS material
  - Fusion bond to silicon cap wafer
  - Grind to target thickness
  - Define standoff for eutectic bond to CMOS wafer
  - Define MEMS accelerometer / gyroscope

Nasiri-Fabrication Process – CMOS wafer

https://invensense.tdk.com/technology/

- CMOS wafer
  - Standard CMOS flow till the last few steps of metallization and passivation

Nasiri-Fabrication Process - Integration

https://invensense.tdk.com/technology/

- CMOS wafer and MEMS wafer Eutectic bonding
  - Vacuum-sealed cavity
  - CMOS-MEMS interconnect through eutectic bonding

Foundry Management - Relationship

- TDK and the foundry partner are working as a team, while respecting each other's technology secrets
  - Customers cannot enter the fab
  - The foundry partner's own engineers cannot bring cell phones into their building
  - The foundry partner has access to TDK's layout, but not design details
- TDK's secrets
  - Design details
  - MEMS design rules
  - Process simulation models
- Foundry's secrets
  - Process integration details
  - Equipment / materials info
  - Process recipes
- Collaborations
  - Process risk related design rules definition
  - Process / design risk assessment
  - Manufacturability review

Foundry Management – New Product Intro

- Risk dashboard
  - List design requirement by the projected market
  - List items with process related risk, root causes, hypothesis, and mitigation plans
  - Project timeline (development time vs. projected market window)
- Tapeout test chip
  - Design split
  - Process split for POR and corner cases
    - Ensure product can meet customer spec with process variations in the fab
  - Test and validation – performance, robustness, reliability
  - Debug
  - Design down selection
- Tapeout product chip
  - Ship to customers

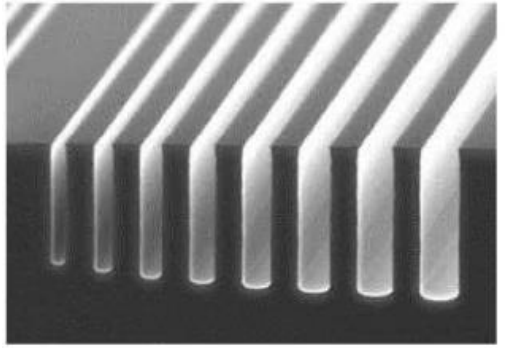
Foundry Management – Tech Dev

- Develop new technology for
  - Lower cost
  - Better performance
  - Quality improvement
- New process technology development requirements
  - Having a target product for interception
  - Process technology development is usually a collaboration between TDK and the foundry
    - New process interested by TDK, but not the foundry → file a patent
    - New process interested by the foundry, but not TDK → no electrical validation
    - New process interested by both, let's make it happen!
  - Manufacturability analysis – process window, equipment capacity, cost, etc.
  - New process module is qualified on existing product with proven design

Foundry Management – Process Predictability

- There is always discrepancy between design and manufactured device
- The DRIE etch defining the actuator is a critical step in the process flow
  - DRIE etch is known to have pattern dependence
  - When the etch profile is different from designers' expectation, the ability to predict performance is compromised
- Foundry team builds process simulation models to predict the device geometry before tapeout
  - Inputs – layout, XSEM data for model calibration
  - Output – virtual metrology to predict the etch profile

DRIE pattern dependency



Introduction to Pattern Dependence Concepts | SEMulator3D Reference © Coventor Inc.

Actuator etch

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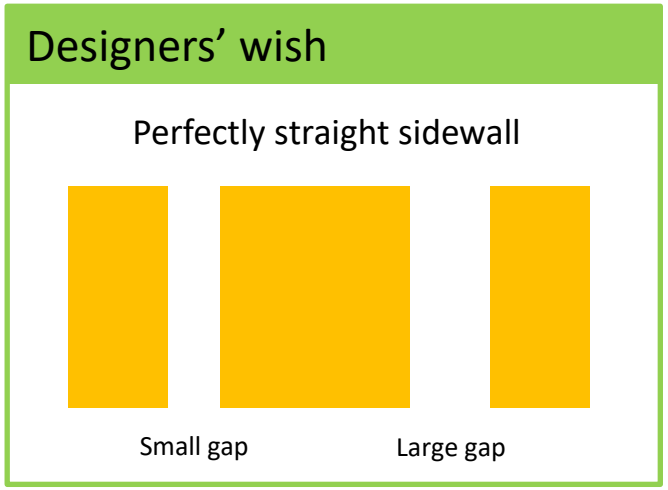

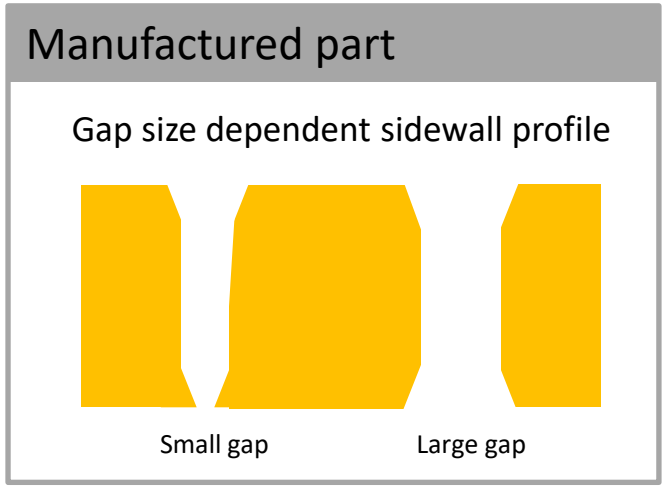

Foundry Management – Failure Analysis

- Failures are usually caught by electrical test
- Wafer pattern on a parameter
  - Trace all wafers with similar pattern
  - Hypothesis table on what-could-go-wrong
  - SPC data look up at foundry
    - In-line and off-line measurement as process control monitor
  - Correlation study with process parameters
  - Tool commonality check
- Lesson learned documentation
  - Problem description
  - Root cause analysis
  - Preventative actions
    - Foundry process modification
    - Design change
    - New design rule enforcement

Lab to Fab Conclusions

Microlab / Nanolab

Goal – Graduation
- Long hours in lab
- Some luck
- Have fun when possible

Startup

Goal – IPO / change the world
- Time to market is critical
- ~1/10 startup can make it to IPO
- < 1/10 will change the world

Major MEMS Company

Goal – Commercial success
- Sensitive to market's new requirements
- Technology development to stay competitive

All stages require hard work and dedication