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Capacitance Parameters for AC Analysis

(SPICE and hand analysis)

EECS 140
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Intrinsic parasitic capacitances

Forward active region: $C_{gs} = \frac{2}{3} WLC_{ox}$ $C_{gd} = 0$

Triode region and small V_{DS}: $C_{gs} = \frac{1}{2} WLC_{ox}$ $C_{gd} = \frac{1}{2} WLC_{ox}$

Extrinsic parasitic capacitances

Gate to drain/source overlap capacitance: $C_{ol} = W \cdot C_{ol}'$

Drain to bulk junction capacitance: $C_{db} = AD \cdot \frac{C_{db0}}{\sqrt{1 + V_{db}/\psi_o}}$

Source to bulk junction capacitance: $C_{sb} = AS \cdot \frac{C_{sb0}}{\sqrt{1 + V_{sb}/\psi_o}}$

Parameter	Symbol	Value
Gate capacitance parameter	C_{ox}	5 fF/μm^2
Overlap capacitance parameter	C_{ol}'	W·0.5 fF/μm
Drain area	AD	W·1μm
Source area	AS	W·1μm
Zero bias junction capacitance	$C_{sb0} = C_{db0}$	1 fF/μm^2
Built-in junction potential	ψ_0	0.5V

Use "capop=0" to get HSPICE to calculate capacitances the same way we do:

```
.model nmos1 nmos vto=1 tox=6.9nm kp=200u lambda=0.1 gamma=0.5 phi=0.6
+ capop=0 cgso=0.5n cgdo=0.5n pb=0.5 cj=1e-3
.model pmos1 pmos vto=-1 tox=6.9nm kp=100u lambda=0.1 gamma=0.5 phi=0.6
+ capop=0 cgso=0.5n cgdo=0.5n pb=0.5 cj=1e-3
```

Then specify AD and AS to get the right Cdb and Csb values:

```
m1 out bias dd dd pmos1 w=200u l=1u AD=2e-10 AS=2e-10
m2 out in  0  0       nmos1 w=100u l=1u AD=1e-10 AS=1e-10
```