MetalMUMPs Design Handbook

a MUMPs® process

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MEMSCAP

Revision 1.0

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Chapter 1
Electroplated Nickel Micromachining Process

1.1. Introduction

The Multi-User MEMS Processes, or MUMPs®, is a commercial program that provides cost-effective, proof-of-concept MEMS fabrication to industry, universities, and government worldwide. MEMSCAP offers three standard processes as part of the MUMPs® program: **PolyMUMPs**, a three-layer polysilicon surface micromachining process: **MetalMUMPs**, an electroplated nickel process; and **SOIMUMPs**, a silicon-on-insulator micromachining process.

The following is a general process description and user guide for MetalMUMPs, which is designed for general-purpose electroplated nickel micromachining of MEMS. Chapter 1 of this document explains the process step-by-step, while Chapter 2 outlines the design rules for the process.

Though this document is geared toward designers who do not have a strong background in microfabrication, it contains information that is useful to all MetalMUMPs users. Regardless of the level of the designer, we strongly recommend all users of PolyMUMPs review this document prior to submitting a design.

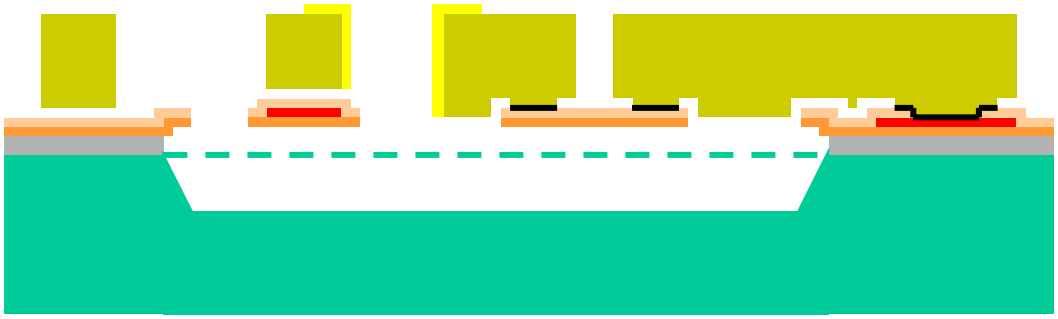


FIGURE 1.1. Cross sectional view of a microrelay fabricated using all layers of the MetalMUMPs process (figure not to scale).

Figure 1.1 is a cross section of a microrelay fabricated with the MetalMUMPs process. This process has the following general features:

1. Electroplated nickel is used as the primary structural material and electrical interconnect layer
2. Doped polysilicon can be used for resistors, additional mechanical structures, and/or cross-over electrical routing
3. Silicon nitride is used as an electrical isolation layer
4. Deposited oxide (PSG) is used for the sacrificial layers
5. A trench layer in the silicon substrate can be incorporated for additional thermal and electrical isolation
6. Gold overplate can be used to coat the sidewalls of nickel structures with a low contact resistance material

The process is designed to be as general as possible, and to be capable of supporting many different designs on a single silicon wafer. Since the process was not optimized with the purpose of fabricating any one specific device, the thicknesses of the structural and sacrificial layers were chosen to suit most users, and the layout design rules were chosen conservatively to guarantee the highest yield possible.

1.2. Process Overview

MetalMUMPs is an electroplated nickel micromachining process derived from work performed at MEMSCAP (JDSU, Cronos, MCNC) throughout the 1990's. This process flow was originally developed for the fabrication of MEMS micro-relay devices based on a thermal actuator technology. The process flow described below is designed to introduce inexperienced users to this micromachining process. The text is supplemented by drawings that show the process flow in the context of building a patented microrelay.

Naming Convention: Lithography levels (i.e. names for each masking level) are typed in upper case. Specific layers of material, such as an oxide, polysilicon, or metal layer, are typed in lower case with the first letter capitalized. For

example POLY refers to the masking level for patterning the polysilicon layer, Poly. Table 2.1 outlines the material layer names, the thickness of each layer, and the lithography levels associated with each layer.

However, be aware that not every upper case word is necessarily a lithography level. Commonly used acronyms such as PSG (PhosphoSilicate Glass), LPCVD (Low Pressure Chemical Vapor Deposition) are uppercase, as are some chemical symbols such as KOH (chemical symbol for potassium hydroxide).

The MetalMUMPs process flow is described below using the naming convention for the various layers.

1. Base wafer: N-type (100) silicon.

2. Isolation Oxide – A 2 um layer of silicon oxide is grown on the wafer surface to provide electrical isolation from the substrate.

3. Oxide 1 – This is a 0.5μm thick PSG layer that acts as a sacrificial release layer. The removal of the Oxide 1 layer at the end of the process releases the Nitride 1 layer (described in # 4). Oxide 1 is lithographically patterned with the first mask level, OXIDE1, and etched. Oxide 1 also defines the regions in which the silicon trench will be formed.

4. Nitride 1 – This is blanket layer of 0.35μm low-stress silicon nitride. Nitride 1 is used in combination with the subsequent Nitride 2 layer for several purposes. The nitride layers provide a protective encapsulation for the polysilicon. The nitride pattern also defines a protective layer on the substrate that determines where Si trench etching occurs (step 12). Third, a released and patterned nitride area may also be used to provide a mechanical linkage between released Metal structures that must be electrically isolated.

5. Poly – This layer is 0.7μm polysilicon film, which is implant doped and annealed to provide consistent electrical properties. The Poly layer is patterned with the second mask level, POLY, and etched. This layer can be used to form resistor elements, mechanical structures, or for electrical cross-over routing.

6. Nitride 2 – This is a second layer of 0.35μm thick low-stress silicon nitride. The combination of Nitride 1 and Nitride 2 layers are lithographically patterned with the third mask level, NITRHOLE, and etched.

7. Oxide 2 – This second sacrificial oxide layer is 1.1μm of PSG. This is removed at the final release step to free the Metal mechanical layer (step 10). Oxide 2 is patterned with the fourth mask level, METANCH, and is wet chemically etched.

8. Anchor Metal – The Oxide 2 patterning step also provides the pattern for the for the metal structure anchors. A liftoff process is used to provide thin layers of Cr and Pt (Anchor Metal) only in the bottom of the Oxide 2 anchors.

9. Plating Base – This layer is a blanket metal layer of 500 nm of Cu protected with a thin Ti layer. The Plating Base layer provides electrical continuity across the wafer for the subsequent Metal electroplating step.

10. Metal - The fifth mask level, METAL, is patterned using a thick resist to form the stencil for the electroplated Metal layer. 20μm of nickel is electroplated into the patterned resist. Subsequently a

0.5μm gold layer is plated on top of the nickel to provide a suitable pad material for wire bonding of external electrical connections. This combination of 20μm nickel and 0.5μm gold forms the Metal layer. The Metal layer serves as the primary mechanical layer and electrical interconnect layer.

11. Sidewall Metal – A final plated metal layer, Sidewall Metal, is a 1-3μm gold layer, plated on selected areas of the sidewall of the Metal layer. This provides a highly reliable low resistance electrical contact and has the effect of shrinking the gaps in adjacent electroplated nickel structures. The process sequence is to first use the sixth mask level, GOLDOVP, to open up an oversized or 'bloated' area in a thick photoresist layer where Sidewall Metal is desired. The Plating Base is removed from any exposed regions using wet chemical etching. The desired resist pattern for Sidewall Metal is then processed with a standard sized or "unbloated" version of GOLDOVP. The 1-3μm thick gold Sidewall Metal layer is then electroplated.

12. The final steps are the release and Si trench etch. The release is a series of wet chemical etches to first remove the Plating Base and then the sacrificial layers and the Isolation oxide layer over the trench areas. Finally, a wet chemical etch of the silicon, using KOH, is used to form a 25μm deep trench in the silicon substrate. This occurs in the areas defined by the OXIDE1 and NITRHOLE masks. This trench provides additional thermal and electrical isolation.

13. The wafers are diced, sorted and shipped to the MetalMUMPs user.

The following pages provide a graphical representation of the process steps.

1.3. MetalMUMPs Process Flow

Oxide 1 Deposited

FIGURE 1.2. A 2μm thick oxide (Isolation Oxide) is grown on the surface of the starting n-type (100) silicon wafer. This is followed by deposition of a 0.5μm thick sacrificial phosphosilicate glass (PSG) layer (Oxide 1).

Oxide 1 Patterned | **Mask Level: OXIDE1**

FIGURE 1.3 The wafers are coated with UV-sensitive photoresist and lithographically patterned by exposing to UV light through the first level mask (OXIDE1), and then developing it. The photoresist in exposed areas is removed, leaving behind a patterned photoresist mask for etching. Wet chemical etching is used to remove the unwanted sacrificial PSG. After the etch, the photoresist is chemically stripped. This method of patterning the wafers with photoresist, etching and stripping the remaining photoresist is used repeatedly in the MetalMUMPs process.

	Substrate		Oxide 1		Poly		Oxide 2		Metal
	Isolation Oxide		Nitride 1		Nitride 2		Anchor Metal		Sidewall Metal
	Photoresist								

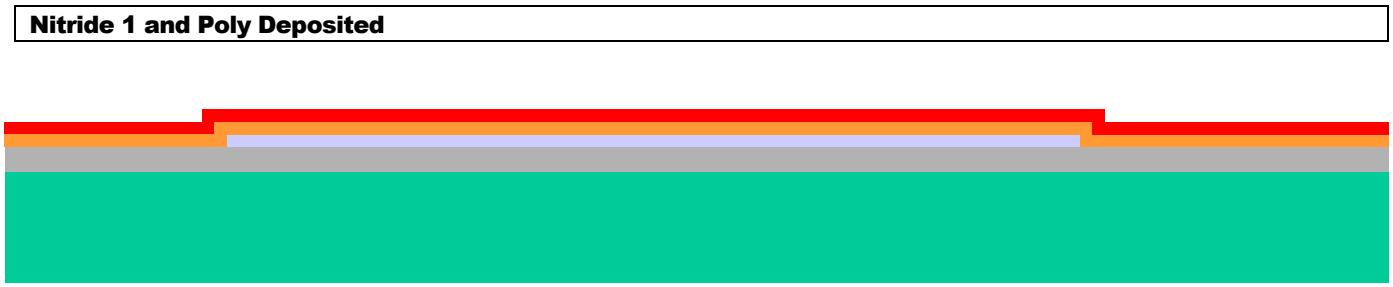


FIGURE 1.4. A 0.35µm layer of silicon nitride (Nitride 1) is deposited, followed immediately by the deposition of a 0.7µm layer of polysilicon (Poly).

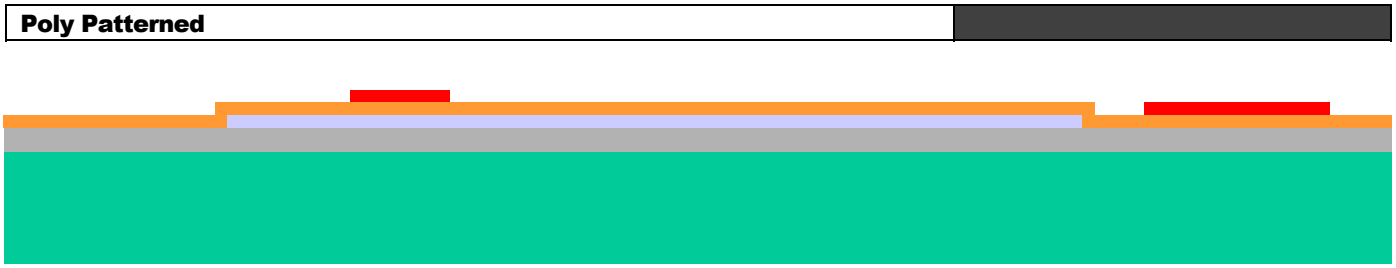


FIGURE 1.5. The wafers are coated with photoresist and the second level (POLY) is lithographically patterned. Reactive ion etching (RIE) is used to remove the unwanted polysilicon. After the etch is completed, the photoresist is removed.

	Substrate		Oxide 1		Poly		Oxide 2		Metal
	Isolation Oxide		Nitride 1		Nitride 2		Anchor Metal		Sidewall Metal
	Photoresist								

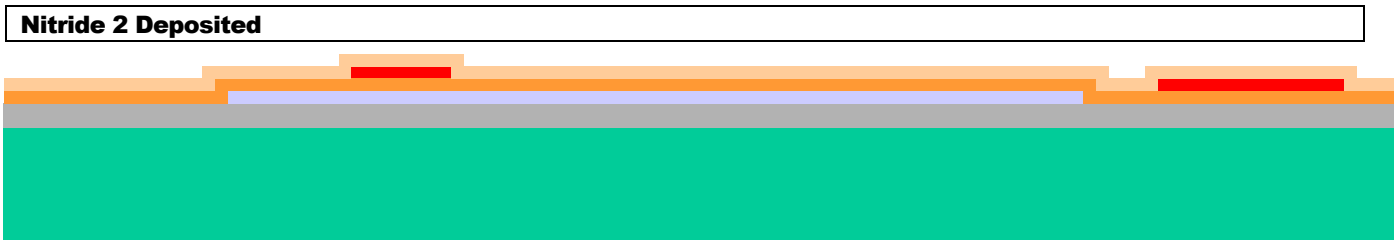


FIGURE 1.6. A second 0.35µm layer of silicon nitride (Nitride 2) is deposited.

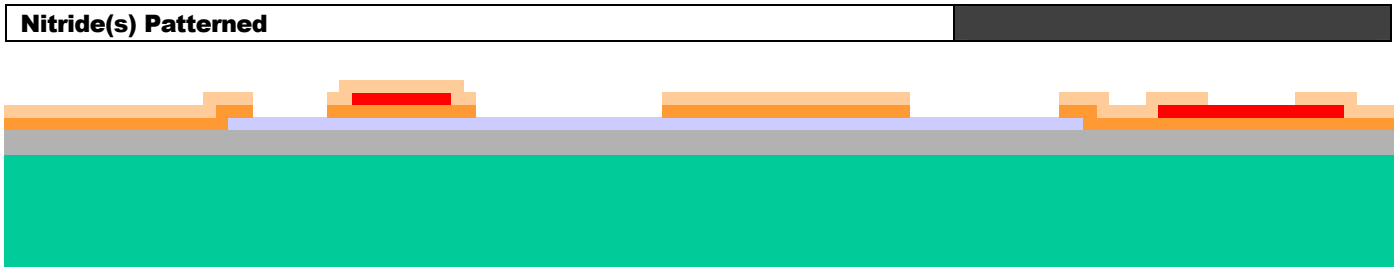


FIGURE 1.7. The wafers are coated with photoresist and the third level (NITRHOLE) is lithographically patterned. RIE etching is performed to remove both Nitride 2 and Nitride 1 from the patterned areas. After the etch is complete, the photoresist is removed. Note: Nitride 1 will remain anywhere NITRHOLE is patterned over Poly.

	Substrate		Oxide 1		Poly		Oxide 2		Metal
	Isolation Oxide		Nitride 1		Nitride 2		Anchor Metal		Sidewall Metal
	Photoresist								

Oxide 2 Patterned and Anchor Metal Deposited	Mask Level: METANCH

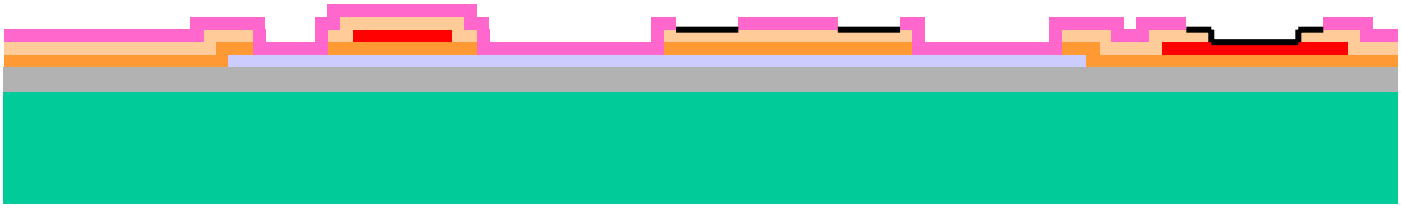


FIGURE 1.9. The wafer is coated with photoresist and the fourth mask level (METANCH) is lithographically patterned. The Oxide 2 is wet etched and a thin metal layer (Anchor Metal) consisting of 10nm Cr + 25nm Pt is deposited. A liftoff process is used to remove the photoresist and leave Anchor Metal only in the bottom of the Oxide 2 openings formed from the METANCH mask level.

Plating Base Deposited and Plating Stencil Patterned	Mask Level: METAL

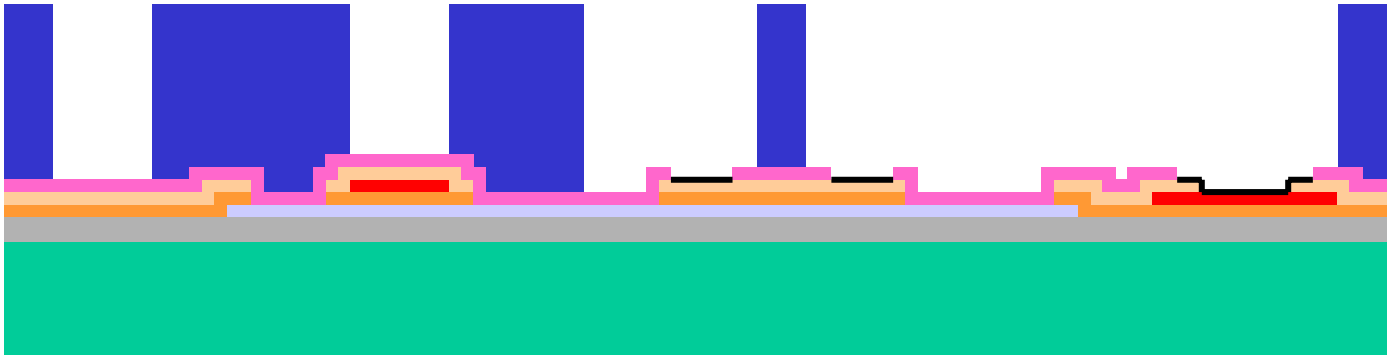


FIGURE 1.10 The Plating base layer, consisting of 500nm Cu + 50nm Ti is deposited. (Not shown). The wafers are coated with a thick layer of photoresist and patterned with the fifth mask level (METAL). This process forms a patterned stencil for the electroplated Metal layer.

	Substrate		Oxide 1		Poly		Oxide 2		Metal
	Isolation Oxide		Nitride 1		Nitride 2		Anchor Metal		Sidewall Metal
	Photoresist								

Metal Plated

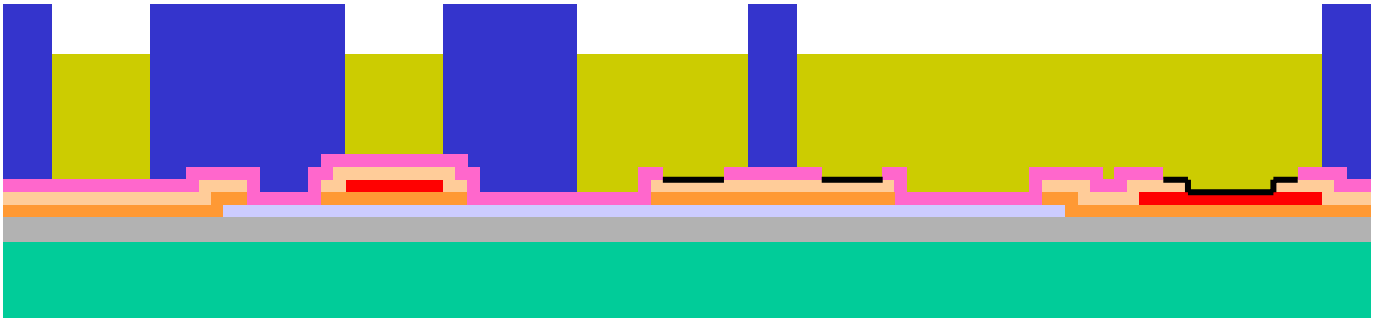


FIGURE 1.11. Nickel is electroplated to a nominal thickness of 20μm into the patterned resist stencil. A 0.5μm gold layer is then immediately electroplated on top of the nickel layer. This forms the Metal layer.

Plating Stencil Removed

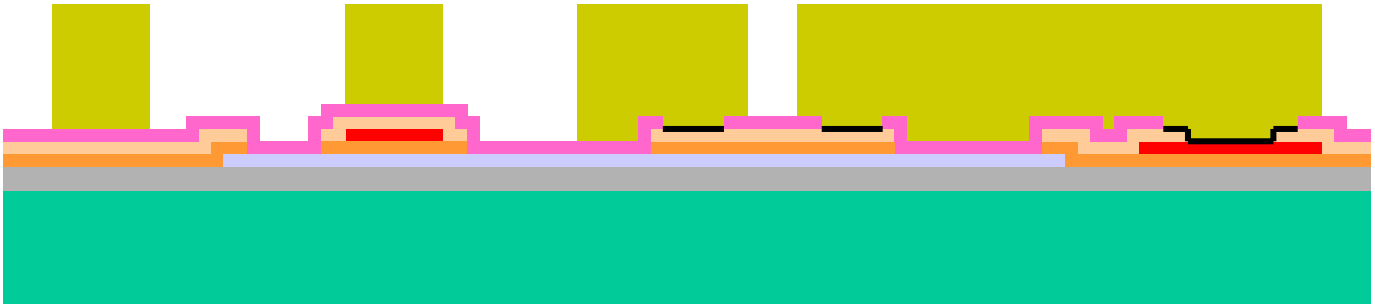


FIGURE 1.12. The photoresist stencil is then chemically removed.

	Substrate		Oxide 1		Poly		Oxide 2		Metal
	Isolation Oxide		Nitride 1		Nitride 2		Anchor Metal		Sidewall Metal
	Photoresist								

Gold Over Plating Stencil Patterned | **Mask Level: GOLDOVP**

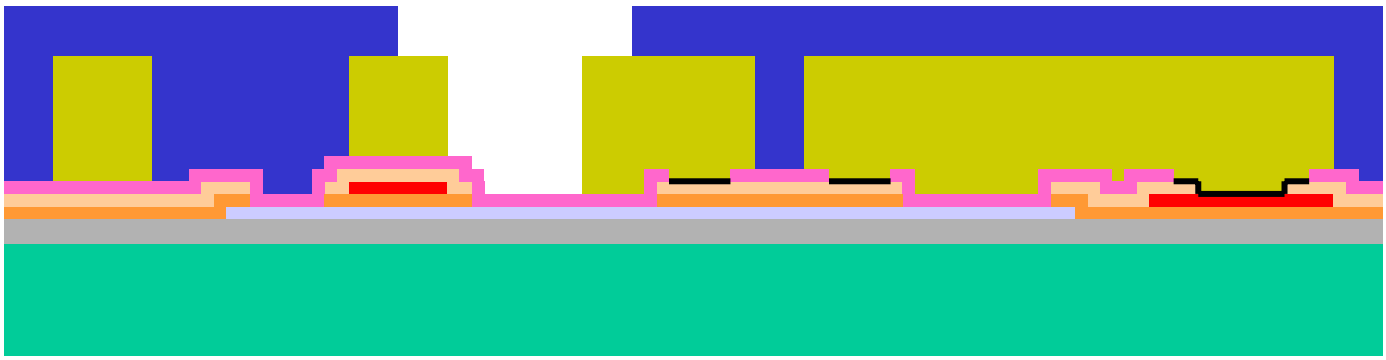


FIGURE 1.13. The wafers are coated with photoresist and patterned with a "bloated" version of the sixth mask level (GOLDOVP) to remove Plating Base in the regions where Sidewall Metal is desired. The Plating Base is chemically removed from the unpatterned regions, and the photoresist is stripped. The wafers are coated with photoresist and patterned with an "un-bloated" version of the sixth mask level (GOLDOVP) to define a resist stencil in the regions of Metal where electroplated Sidewall Metal is desired.

Gold Over Plating

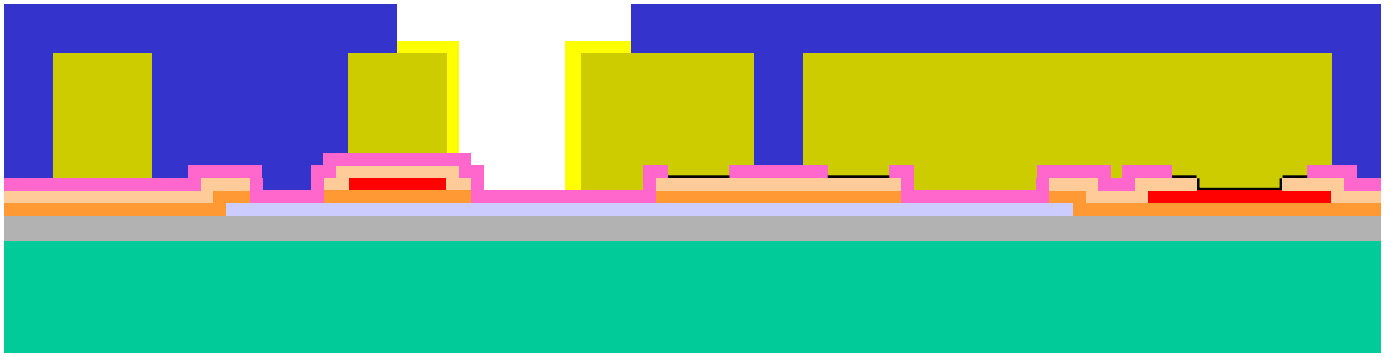


FIGURE 1.14. A 1-3µm gold layer (Sidewall Metal) is electroplated using the GOLDOVP photoresist mask as a stencil.

	Substrate		Oxide 1		Poly		Oxide 2		Metal
	Isolation Oxide		Nitride 1		Nitride 2		Anchor Metal		Sidewall Metal
	Photoresist								

Gold Over Plating Stencil Removed

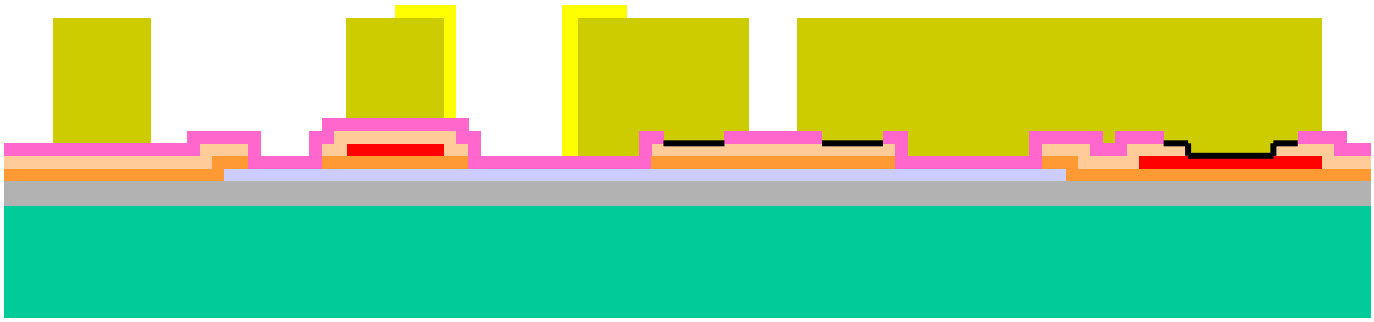


FIGURE 1.15. The GOLDOVP resist stencil is stripped.

Plating Base and Sacrificial Oxides Removed

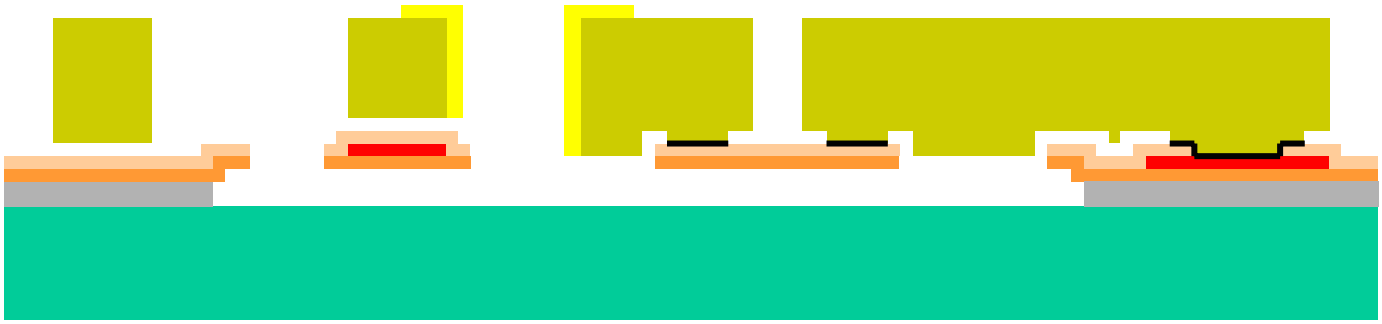


FIGURE 1.16. Plating Base is chemically stripped in the first step of the release process. In the second step of the release process, a 49% HF solution is used to remove the PSG sacrificial layers (Oxide 1 and Oxide 2) and the Isolation Oxide layer over the trench areas.

	Substrate		Oxide 1		Poly		Oxide 2		Metal
	Isolation Oxide		Nitride 1		Nitride 2		Anchor Metal		Sidewall Metal
	Photoresist								

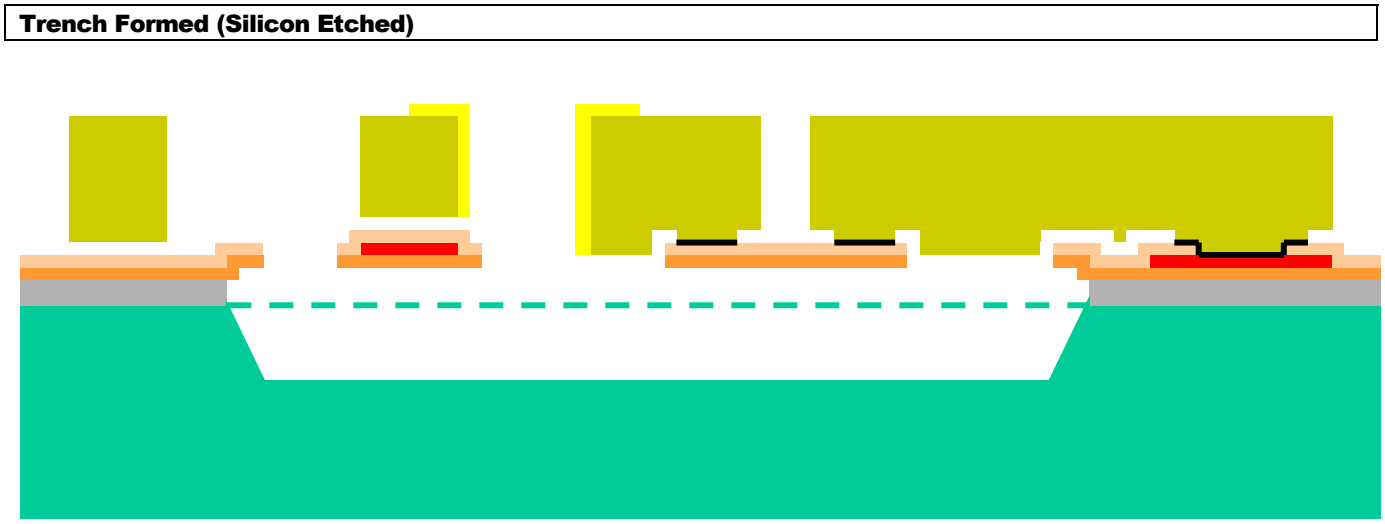


FIGURE 1.17. In the final step of the release process, a KOH silicon etch is used to form a 25µm deep trench in the silicon substrate in the areas defined by the OXIDE1 and NITRHOLE mask levels.

	Substrate		Oxide 1		Poly		Oxide 2		Metal
	Isolation Oxide		Nitride 1		Nitride 2		Anchor Metal		Sidewall Metal
	Photoresist								

Chapter 2
MetalMUMPs Design Rules and Considerations

2.1. Introduction

The purpose of the design rules is to ensure the greatest possibility of successful fabrication. The rules have evolved through process development and the experience of the MEMSCAP staff. The design rules are a set of requirements and advisements that are defined by the limits of the process (i.e. the stable process window) that in turn is defined by the capabilities of the individual process steps. This section of the document describes the design rules that exist for the MetalMUMPs electroplated nickel micromachining process.

Design rules in the document define the minimum feature sizes and spaces for all levels and minimum overlap and spacing between relevant levels. The **minimum line widths and spaces are mandatory rules**. Mandatory rules are given to ensure that all layouts will remain compatible with MEMSCAP lithographic process tolerances. Violation of minimum line/space rules will result in missing, undersized, oversized or fused features. Minimum overlap (enclosure, cut-in and cut-out rules) requirements reduce the effect of large topographies and prevent unnecessary etching of underlying layers. Minimum spacing between levels guarantees that features of two different levels can be delineated by photolithography and etch. **Please note: The minimum geometry allowed should not be confused with the nominal geometry a designer uses. Minimum geometries should only be used where absolutely necessary.** When size is not an issue, the feature should be designed larger than the minimum allowed value.

Finally, there are a few things to keep in mind regarding naming conventions. Lithography levels (i.e. names for each masking level) will be written in upper case. When referring to a specific layer of material, be it oxide, polysilicon, or metal, the material will be typed in lower case with the first letter capitalized. For example POLY refers to the masking level for patterning the polysilicon layer, Poly. Table 2.1 outlines the material layer names, thicknesses and the lithography levels associated with those layers.

Material Layer	Thickness (μm)	Lithography Level Name	Lithography Level Purpose	Comments
Isolation Oxide	2.0			2.0μm thermal oxide
Oxide 1	0.5	OXIDE1	Define trench; release Nitride	0.5μm PSG
Nitride 1	0.35			0.35μm low-stress silicon nitride
Poly	0.7	POLY (HOLP)	Pattern Poly	0.7μm doped polysilicon
Nitride 2	0.35	NITRHOLE	Define areas where Nitride is removed. Define trench. Open hole for electrical contact between Metal and Poly	Patterns both Nitride 2 and Nitride 1
Oxide 2	1.1	METANCH	Open holes to anchor Metal to Nitride or Poly. Open holes for thin metal traces of Anchor Metal	1.1μm PSG
Anchor Metal	0.035	METANCH		10nm Cr + 25nm Pt
Plating Base	0.55			500nm Cu + 50nm Ti
Metal	20.5	METAL (HOLM)	Pattern Metal	20μm Ni + 0.5μm Au
Sidewall Metal	1.0 - 3.0	GOLDOVP	Define area for Sidewall Metal and pattern Sidewall Metal	1-3μm Au

TABLE 2.1. Layer names, thicknesses and lithography levels

***NOTE: The "substrate" designation in Table 2.1 and Table 2.2 refers to a mechanical attachment to the Isolation Oxide layer grown on the silicon wafer surface. It is NOT an electrical connection to the underlying silicon wafer.**

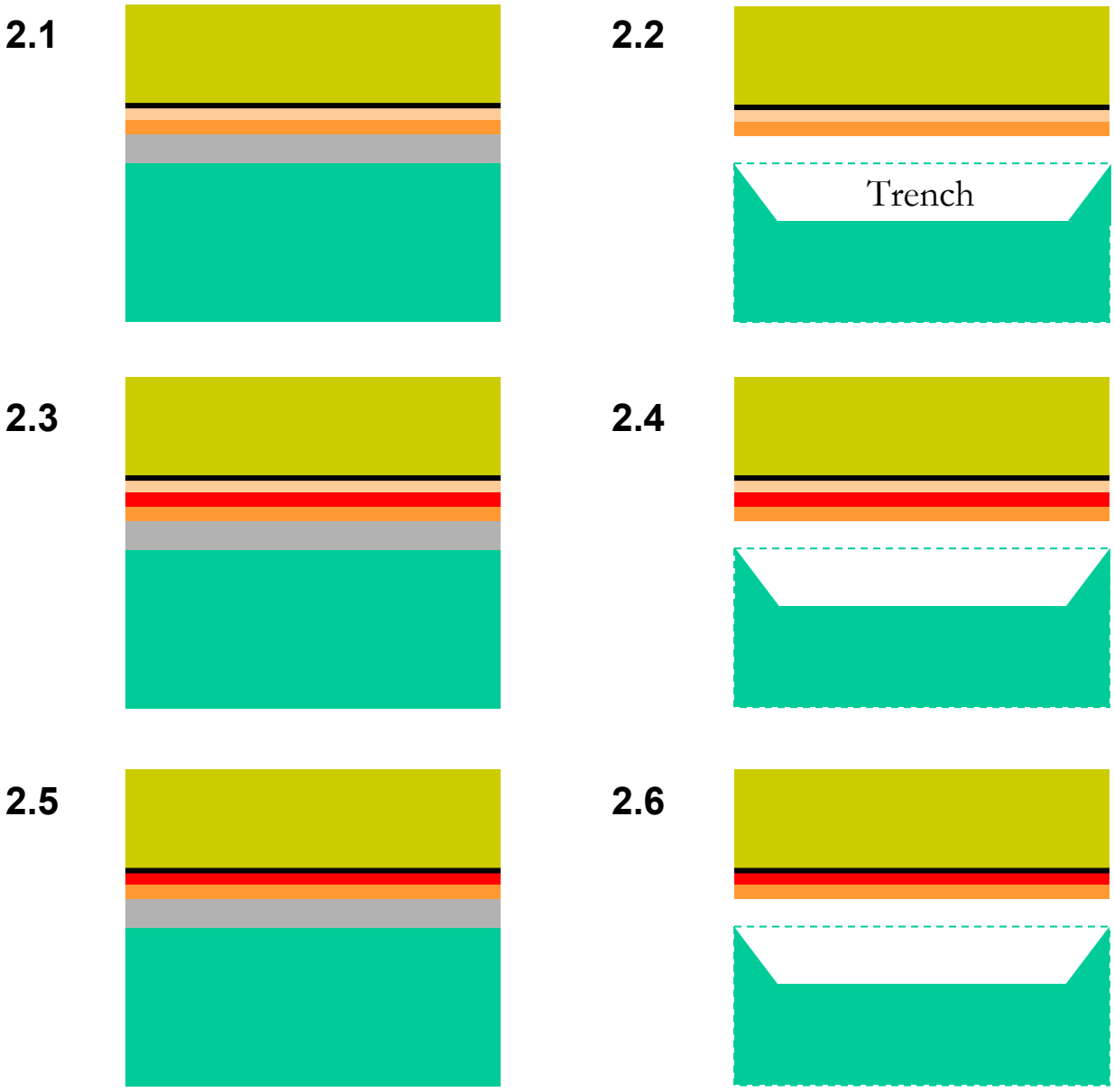
2.2. Allowable Layer Combinations

Table 2.2 outlines the allowable layer combinations that are available in the MetalMUMPs process. This information is presented in a "Truth Table" format to provide the designer with a quick reference for identifying which layers are to be present for building various structures. Figures 2.1-2.20 provide a visual cross-section representation of the structures that can be realized through the allowable layer combinations.

Structure	Type	Oxide 1	Nitride 1	Poly	Nitride 2	Oxide 2	Anchor Metal	Metal	Drawing Ref.	Comments
Attached Metal (Plated Nickel)	to Nitride2/Nitride1/Substrate (fixed)	N	Y	N	Y	N	Y	Y	2.1	Metal anchored to Substrate through Nitride
	to Nitride2/Nitride1 (released)	Y	Y	N	Y	N	Y	Y	2.2	Metal attached to released Nitride
	to Nitride2/Poly/Nitride1/Substrate (fixed)	N	Y	Y	Y	N	Y	Y	2.3	Metal anchored to Substrate through Nitride with embedded Poly
	to Nitride2/Poly/Nitride1 (released)	Y	Y	Y	Y	N	Y	Y	2.4	Metal attached to released Nitride with embedded Poly
	to Poly/Nitride1/Substrate (fixed)	N	Y	Y	N	N	Y	Y	2.5	Metal anchored to Substrate through Poly/Nitride (electrical contact to Poly)
	to Poly/Nitride1 (released)	Y	Y	Y	N	N	Y	Y	2.6	Metal attached to released Poly (electrical contact to Poly)
Free Metal over air (Plated Nickel)	over Trench in Substrate	Y	N	N	N	Y	N	Y	2.7	Released Metal
	over Nitride2/Nitride1/Substrate	N	Y	N	Y	Y	N	Y	2.8	Released Metal over fixed Nitride
	over Nitride2/Nitride1/Trench	Y	Y	N	Y	Y	N	Y	2.9	Released Metal over released Nitride
	over Nitride2/Poly/Nitride1/Substrate	N	Y	Y	Y	Y	N	Y	2.10	Released Metal over fixed Poly embedded in Nitride
	over Nitride2/Poly/Nitride1/Trench	Y	Y	Y	Y	Y	N	Y	2.11	Released Metal over released Poly embedded in Nitride
No Metal	Nitride2/Nitride1/Substrate (fixed)	N	Y	N	Y	Y	N	N	2.12	Nitride in "field" regions
	Nitride2/Nitride1 (released)	Y	Y	N	Y	Y	N	N	2.13	Released Nitride
	Nitride2/Poly/Nitride1/Substrate (fixed)	N	Y	Y	Y	Y	N	N	2.14	Embedded Poly anchored to substrate
	Nitride2/Poly/Nitride1 (released)	Y	Y	Y	Y	Y	N	N	2.15	Embedded Poly released
	No films (trench only)	Y	N	N	N	Y	N	N	2.16	Trench with no films over it
Thin Metal Traces (Anchor Metal)	on Nitride2/Nitride1/Substrate (fixed)	N	Y	N	Y	N	Y	N	2.17	Thin metal trace on top of anchored nitride
	on Nitride2/Nitride1 (released)	Y	Y	N	Y	N	Y	N	2.18	Thin metal trace on top of released nitride
	on Nitride2/Poly/Nitride1/Substrate (fixed)	N	Y	Y	Y	N	Y	N	2.19	Thin metal trace on top of anchored nitride with embedded poly
	on Nitride2/Poly/Nitride1 (released)	Y	Y	Y	Y	N	Y	N	2.20	Thin metal trace on top of released nitride with embedded poly

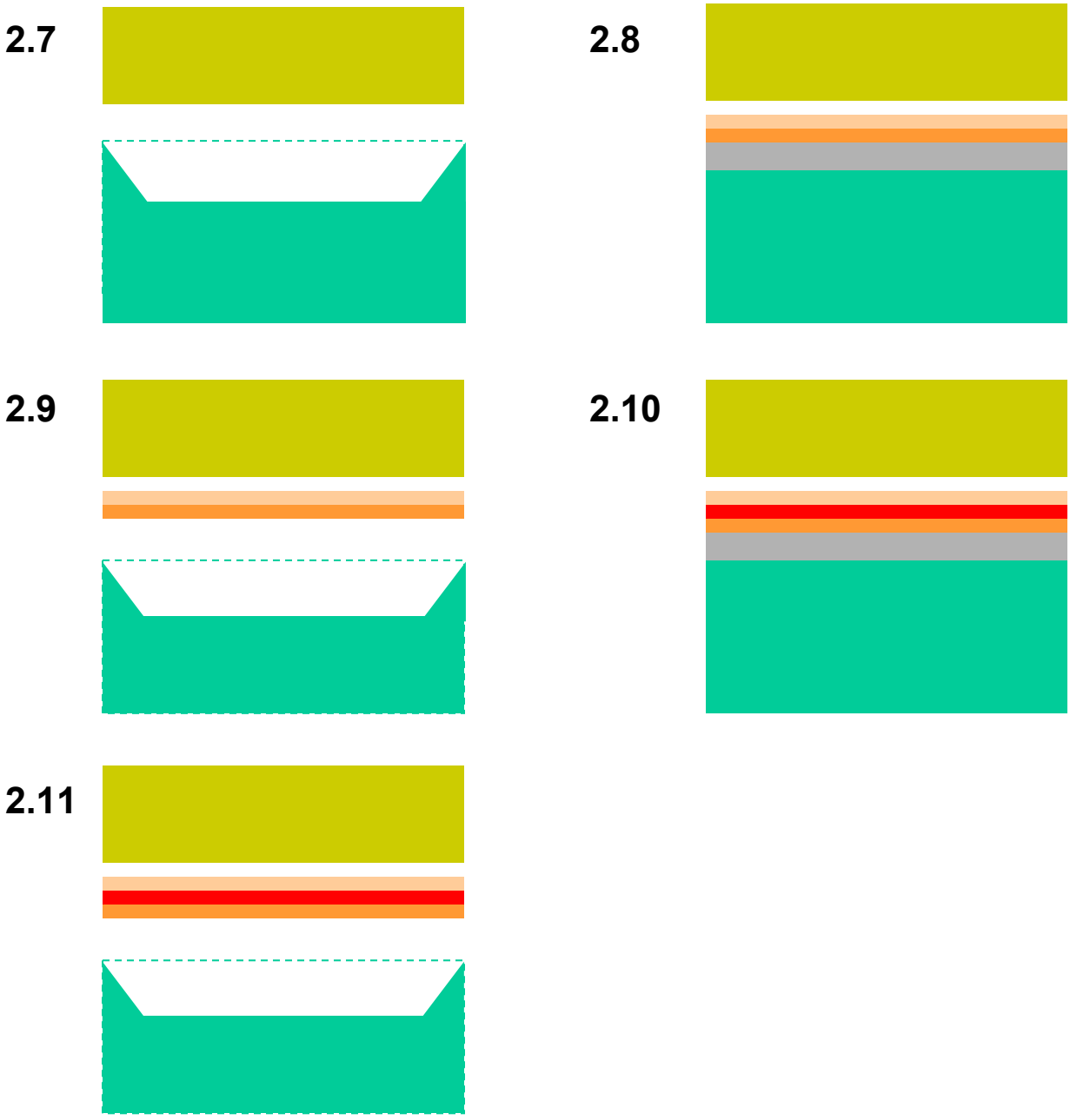
NOTES:
A. Nitride 1 and Anchor Metal are not independently defined; Nitride 1 is defined by the combination of Nitride2 and Poly (Nitride 1 is present unless both Nitride2 and Poly are removed); Anchor Metal is defined by the opposite of Oxide 2.
B. Although other layer combinations can be drawn, these are the only combinations allowed by the MetalMUMPs process

TABLE 2.2 Allowable Layer Combinations and Associated Structures in MetalMUMPs.



FIGURES 2.1-2.6 Cross-Sectional Representations of Attached Metal (Nickel) Structures (from Table 2.2).

	Substrate		Oxide 1		Poly		Oxide 2		Metal
	Isolation Oxide		Nitride 1		Nitride 2		Anchor Metal		Sidewall Metal
	Photoresist								

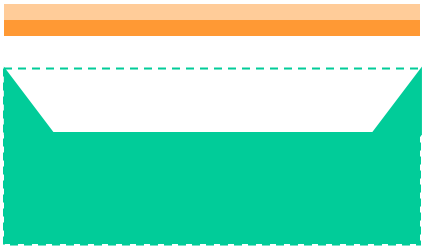


FIGURES 2.7-2.11 Cross-Sectional Representations of Free Metal (Nickel) Structures (from Table 2.2)

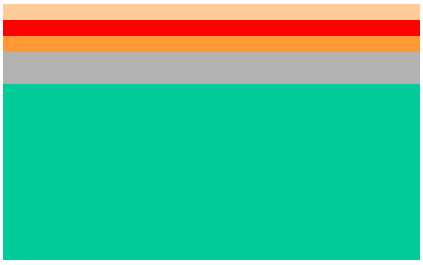
	Substrate		Oxide 1		Poly		Oxide 2		Metal
	Isolation Oxide		Nitride 1		Nitride 2		Anchor Metal		Sidewall Metal
	Photoresist								

2.12

2.13



2.14



2.15

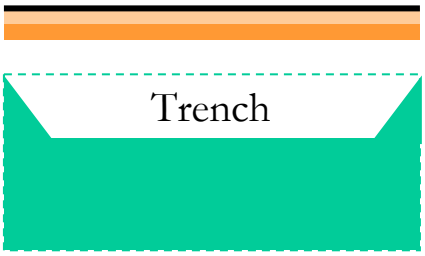
2.16

FIGURES 2.12-2.16 Cross-Sectional Representations of No Metal Structures (from Table 2.2)

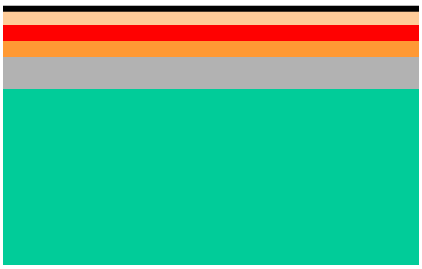
	Substrate		Oxide 1		Poly		Oxide 2		Metal
	Isolation Oxide		Nitride 1		Nitride 2		Anchor Metal		Sidewall Metal
	Photoresist								

2.17

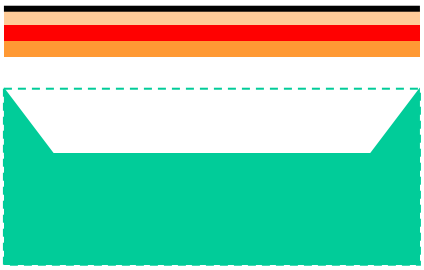
2.18



2.19



2.20



FIGURES 2.17-2.20 Cross-Sectional Representations of Thin Metal Trace Structures (from Table 2.2)

	Substrate		Oxide 1		Poly		Oxide 2		Metal
	Isolation Oxide		Nitride 1		Nitride 2		Anchor Metal		Sidewall Metal
	Photoresist								

2.3. Design Rules

The design rules for the MetalMUMPs process are described both in tabular form and in schematic drawings. The tables list the rules and gives references to the specific figure in which the rule is described.

Table 2.3 lists the cross-reference between MEMSCAP descriptive name, the CIF name and the GDS level number. These are the level names and numbers referred to in the process guide and in any communications you may have with MEMSCAP layout support. Please adopt this naming scheme on your own layout system to minimize confusion when you transfer your data file to MEMSCAP for fabrication. The table also lists the nominal feature/space and the minimum feature and space allowable for that level. These minimum features and spacings are **mandatory** rules.

Mnemonic level name	CIF level name	GDS level number	Min. feature (μm)	Min. space (μm)
OXIDE1	OX1	10	20	20
POLY	POLY	20	5	5
NITRHOLE	NITR	30	5	5
METANCH	ANCH	40	50	10
METAL	METL	50	8	8
GOLDOVP	OVP	60	50	50
HOLEP	HOLP	21	5	5
HOLEM	HOLM	51	8	8

TABLE 2.3. MEMSCAP level name, CIF and GDSII™ level designation, and nominal and minimum features and spaces for each level.

The hole layers (HOLEP and HOLEM) for POLY and METAL, respectively, are shown as separate levels in order to make layout of POLY and METAL easier. The principal purpose of these holes is to provide shorter release etch paths under large Poly and Metal features. The secondary purpose is to provide a simple way to "extract" holes from a light field level. The drawing of holes in a large digitized (drawn) level can be difficult, or even impossible with some layout systems. MEMSCAP has chosen to define unique levels for drawing holes to simplify this process. You need only draw the physical Poly or Metal structure without the holes, then draw (digitize) the desired etch hole on the corresponding HOLE level and MEMSCAP will superimpose the two levels. Table 2.1 and Table 2.3 indicate the proper correspondence between layers. Since hole levels are actually part of their corresponding light field levels (e.g. HOLEM is part of METAL), all holes are subject to the same dimension and alignment rules as the corresponding level. **Do not use the hole layers to define geometries other than etch holes!**

It should be noted that the photo masking process used by MEMSCAP is capable of rendering arcs and non-rectangular polygons. You are welcome and encouraged to include non-Manhattan geometries as part of your submission. Keep in mind, however, that the masks are printed with a 0.25 μm spot size and all features are limited by this registration. To minimize vertex snapping errors in the fracturing of the data, please use a 0.25 micron grid in layout and avoid rotating cells.

2.3.1. Rule Nomenclature

This document uses nomenclature that may not be familiar to some users. The nomenclature is based on Boolean operators that are used in a design rule checker. There are two basic operators used to describe the rules: enclose and spacing. The following diagrams explain the nomenclature and describe the operators and rule.

Enclose L2 by L1 (Figure 2.3.1) This operator defines a boundary by which layer L1 must surround layer L2. The boundary has an associated minimum value, A.

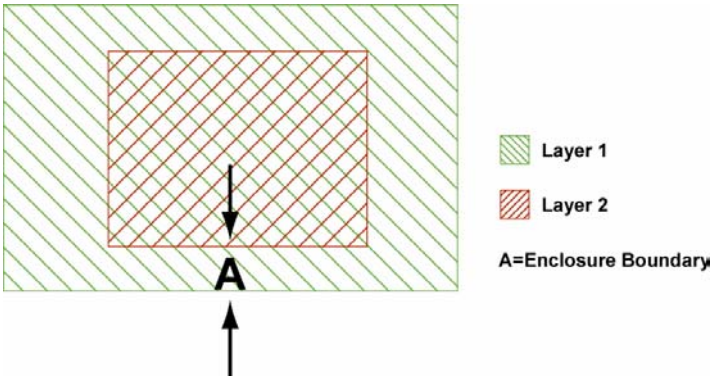


FIGURE 2.3.1. Enclose Layer2 by Layer1. A = minimum boundary dimension.

Spacing L1 to L2 (Figure 2.3.2). The operator defines the spacing between two layers L1 and L2. The spacing has an associated minimum value, B.

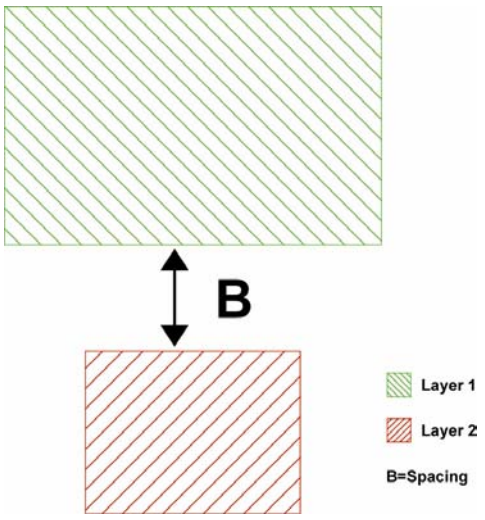


FIGURE 2.3.2. Spacing Layer1 to Layer2. B = minimum spacing

2.3.2. Level to Level Design Rules

The level to level design rules are listed in Table 2.4. The rules are given in each line of the table along with a figure number and a rule letter. Figures 2.3.3 through 2.3.8 are cross sections and plan views of various "common" design structures that illustrate the rules. The figures are drawn with the structures released, after Oxide 1 and Oxide 2 have been removed and the trench has been formed. The rule letters point out which dimensions on the plan view pertain to the specific rule, and the corresponding verbal explanation of that rule. Please note that the drawings show how the films relate to each other up to that point of processing. For clarity, the drawings do not necessarily represent true or completed structures. Also of importance, the plan views show the drawn (digitized) layout and cross sections show the resulting structures. This should help you better visualize the rules in layout form.

Rule	Rule Letter	Figure #	Min. Value (μm)
OXIDE1 enclose NITRHOLE	A	2.3.5 – 2.3.7	5.0
POLY enclose NITRHOLE	B	2.3.4	5.0
NITRHOLE space to POLY	C	2.3.7	5.0
METAL enclose NITRHOLE	D	2.3.4	25.0
METAL enclose METANCH	E	2.3.3 – 2.3.7	5.0
Lateral Etch Holes space in Nitride	F	2.3.8	≤ 100.0 (max. value)
Lateral Etch Holes space in Metal	G	2.3.8	≤ 100.0 (max. value)

TABLE 2.4. Level to Level Design Rules

- **Rule A ensures proper placement of the NITRHOLE layer with respect to OXIDE1 for trench formation.**
- **Rules B, C, and D define proper enclosure of the Poly layer to ensure that the polysilicon is protected during the KOH etching that forms the trench in the silicon substrate.**
- **Rule D also ensures that the Metal (Ni) remains anchored during the removal of the plating base layer.**
  (It sufficiently allows for undercutting during the wet copper etching that is used to strip the plating base).
- **Rule E ensures that the Metal properly overlaps anchor and via holes.**
- **Rules F ensures the release of large Nitride features (when desired).**
- **Rules G ensures the release of large Metal (Nickel) features (when desired).**

NOTE: The design rules governing the gold overplate layer (GOLDOVP) will be described separately in section 2.3.3.

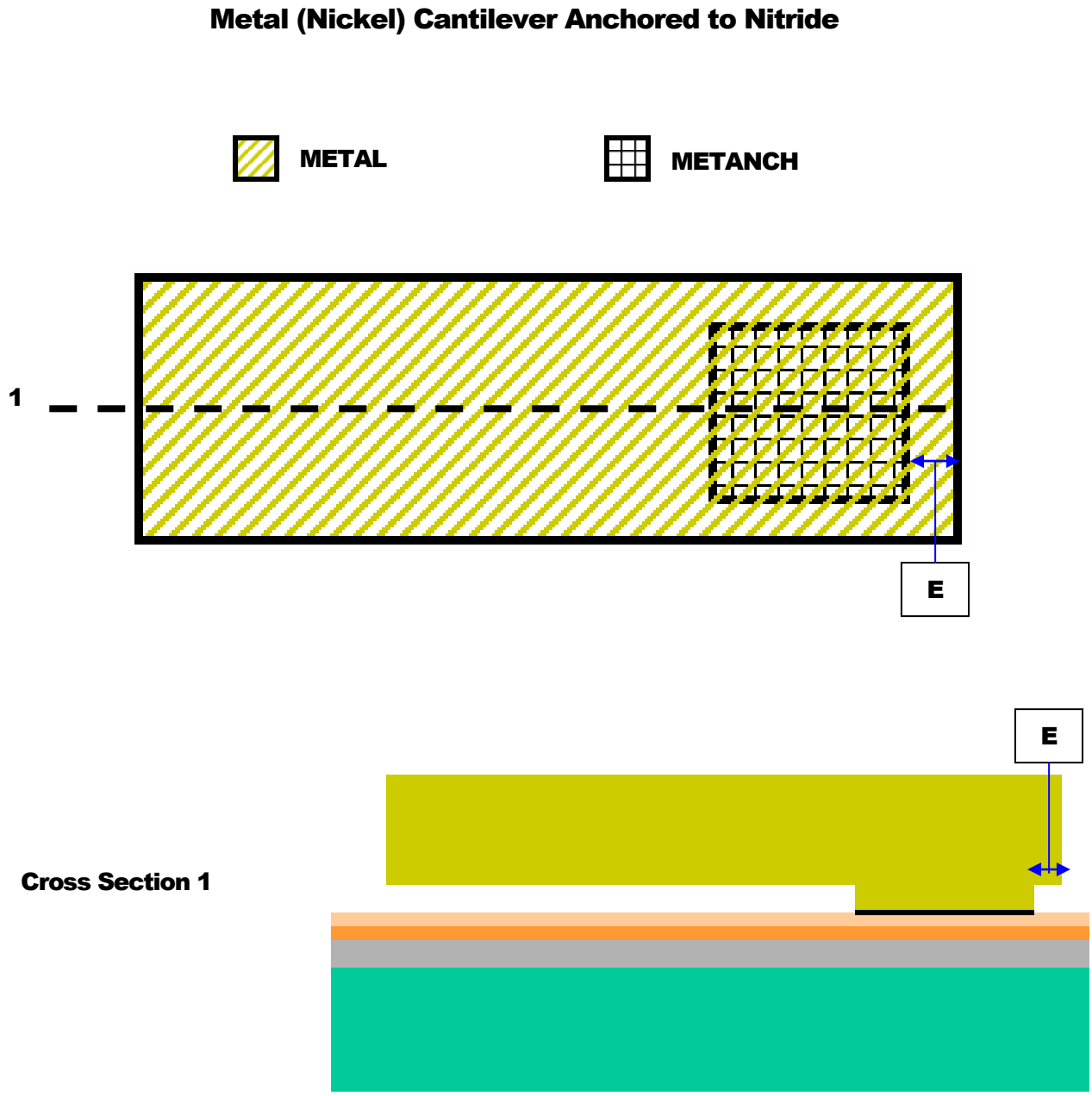


FIGURE 2.3.3.
E: METAL enclose METANCH > 5.0μm. The amount that Metal must extend beyond the edge of METANCH to ensure complete coverage of the hole.

	Substrate		Oxide 1		Poly		Oxide 2		Metal
	Isolation Oxide		Nitride 1		Nitride 2		Anchor Metal		Sidewall Metal
	Photoresist								

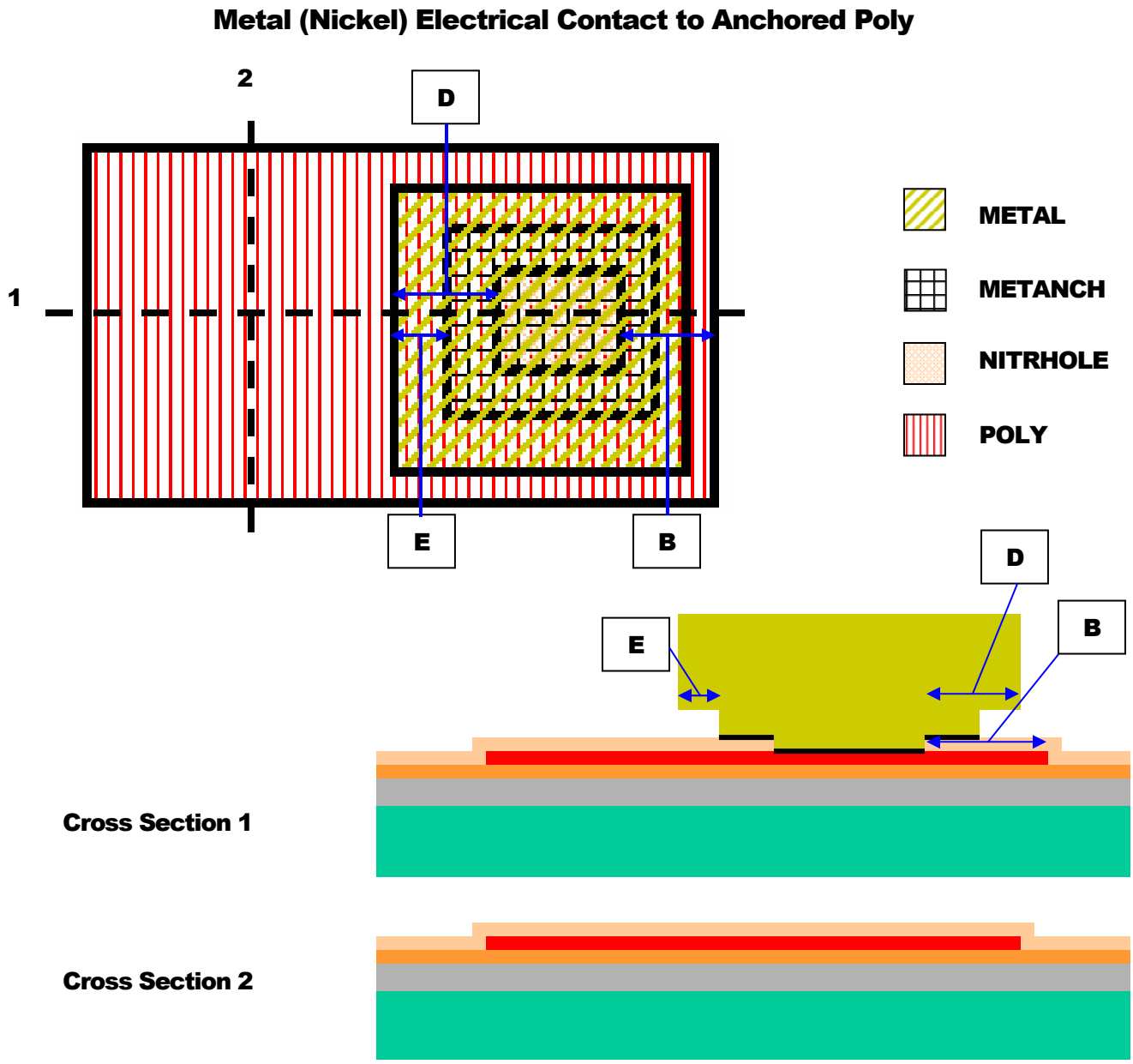


FIGURE 2.3.4.

B: POLY enclose NITRHOLE > 5.0µm. The amount that Poly must extend beyond the edge of NITRHOLE to ensure protection of the poly during the KOH trench etching.

D: METAL enclose NITRHOLE > 25.0µm. The amount that Metal must extend beyond the edge of METANCH to ensure complete coverage of the hole.

E: METAL enclose METANCH > 5.0µm. The amount that Metal must extend beyond the edge of METANCH to ensure complete coverage of the hole.

	Substrate		Oxide 1		Poly		Oxide 2		Metal
	Isolation Oxide		Nitride 1		Nitride 2		Anchor Metal		Sidewall Metal
	Photoresist								

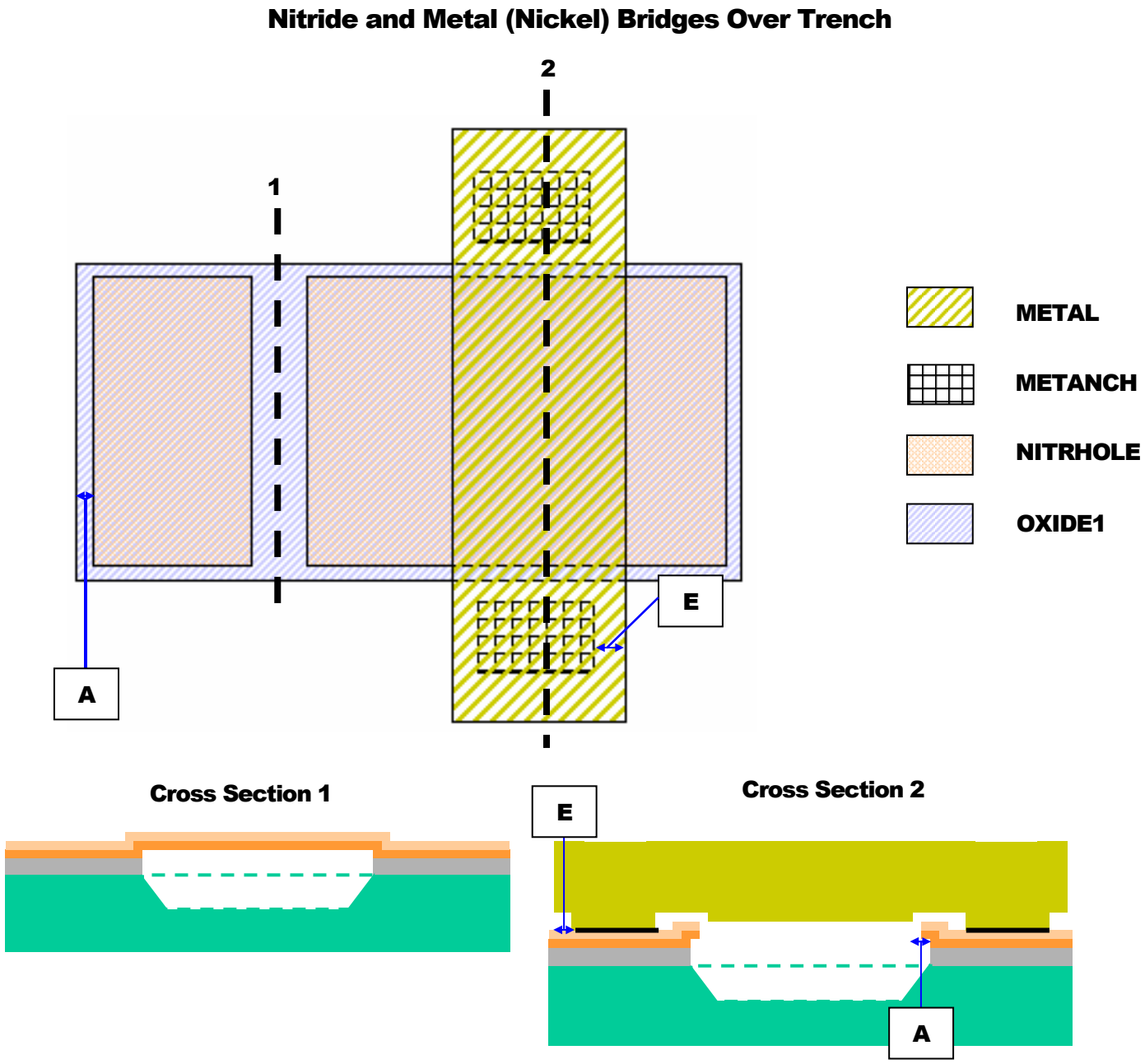


FIGURE 2.3.5.

A: OXIDE1 enclose NITRHOLE > 5.0μm. The amount that Oxide 1 must extend beyond the edge of NITRHOLE to ensure proper trench formation

E: METAL enclose METANCH > 5.0μm. The amount that Metal must extend beyond the edge of METANCH to ensure complete coverage of the hole.

	Substrate		Oxide 1		Poly		Oxide 2		Metal
	Isolation Oxide		Nitride 1		Nitride 2		Anchor Metal		Sidewall Metal
	Photoresist								

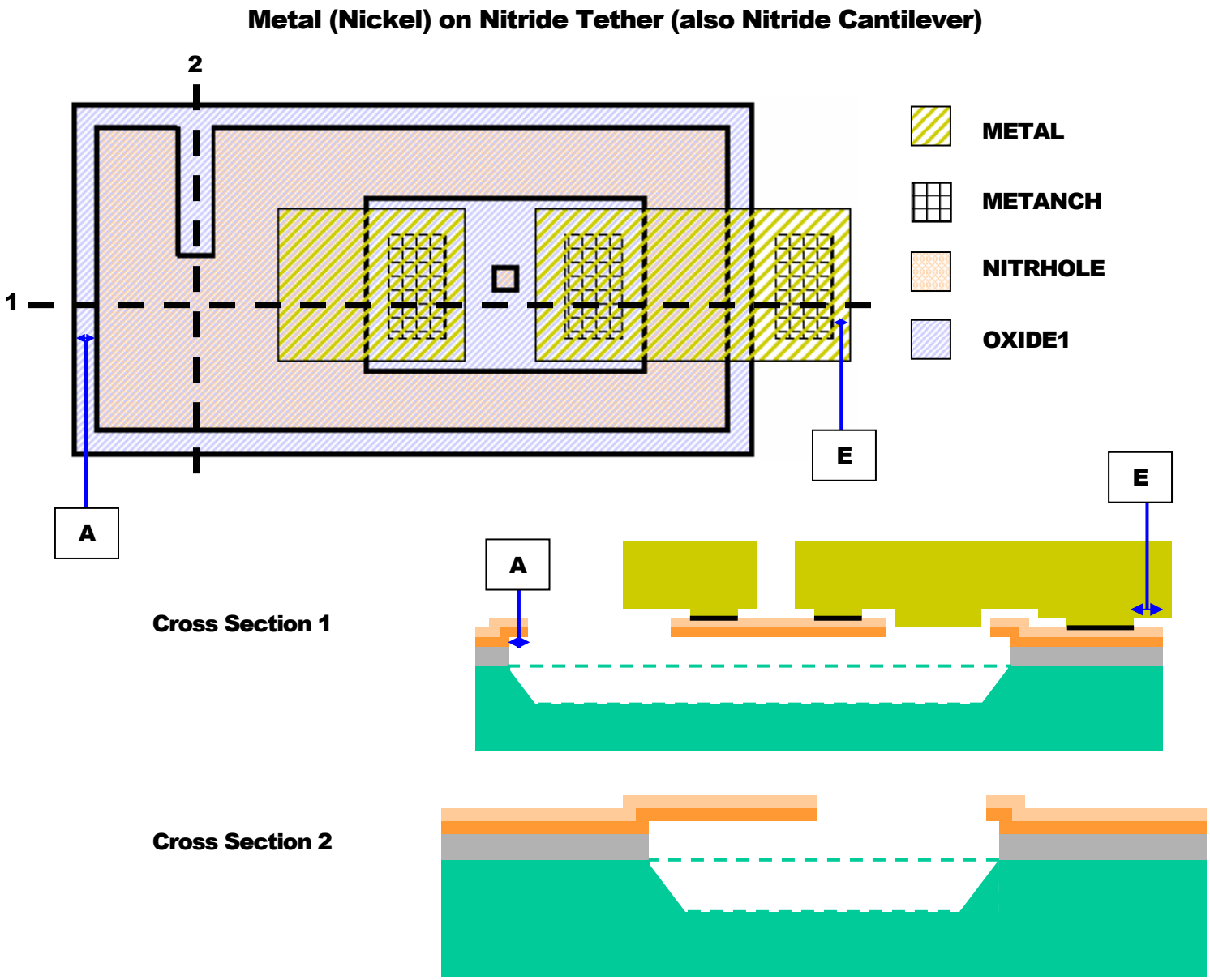


FIGURE 2.3.6.

A: OXIDE1 enclose NITRHOLE > 5.0µm. The amount that Oxide 1 must extend beyond the edge of NITRHOLE to ensure proper trench formation

E: METAL enclose METANCH > 5.0µm. The amount that Metal must extend beyond the edge of METANCH to ensure complete coverage of the hole.

	Substrate		Oxide 1		Poly		Oxide 2		Metal
	Isolation Oxide		Nitride 1		Nitride 2		Anchor Metal		Sidewall Metal
	Photoresist								

Metal (Nickel) Bridge Crossing Released Poly with Etch Holes

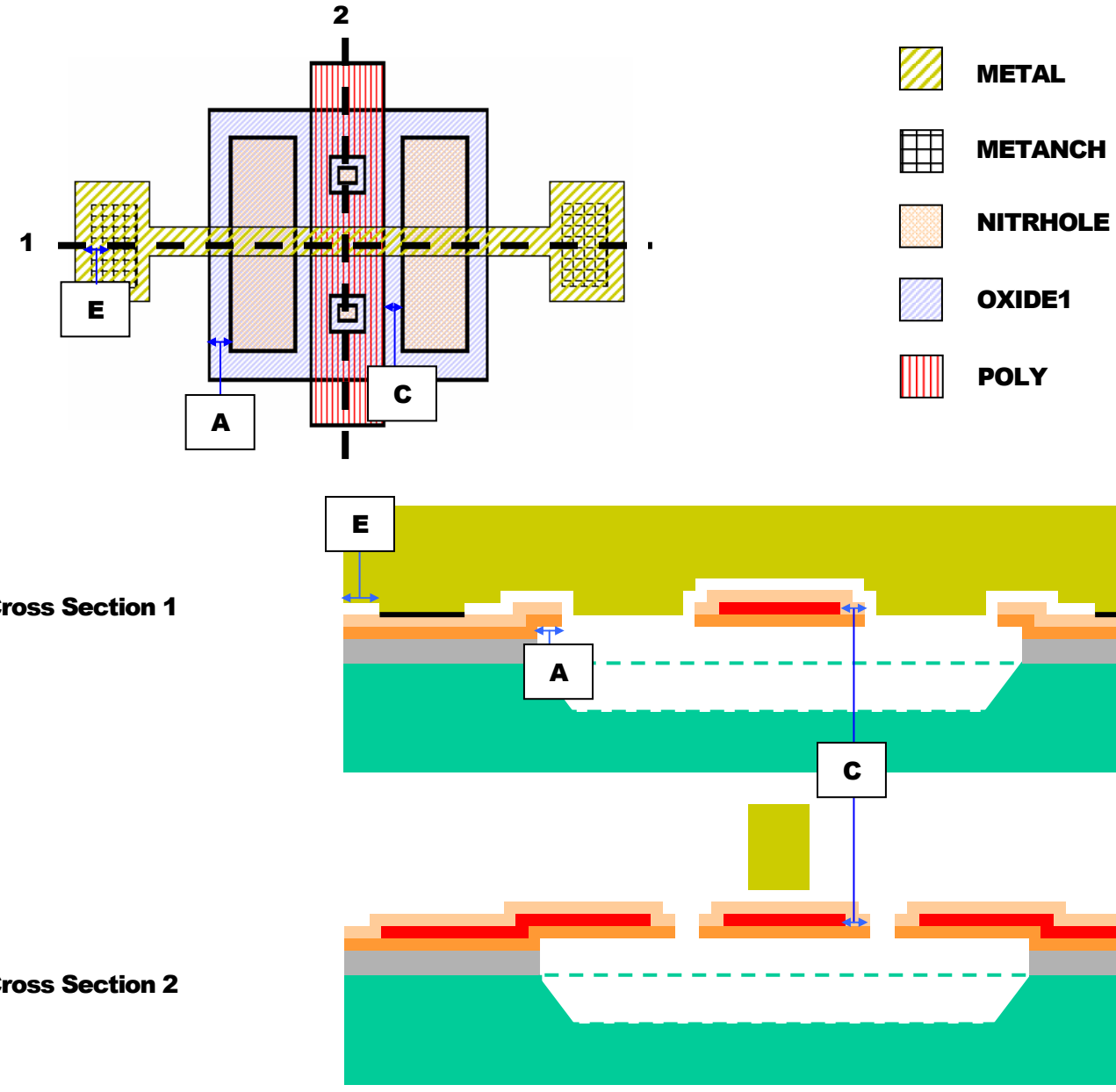


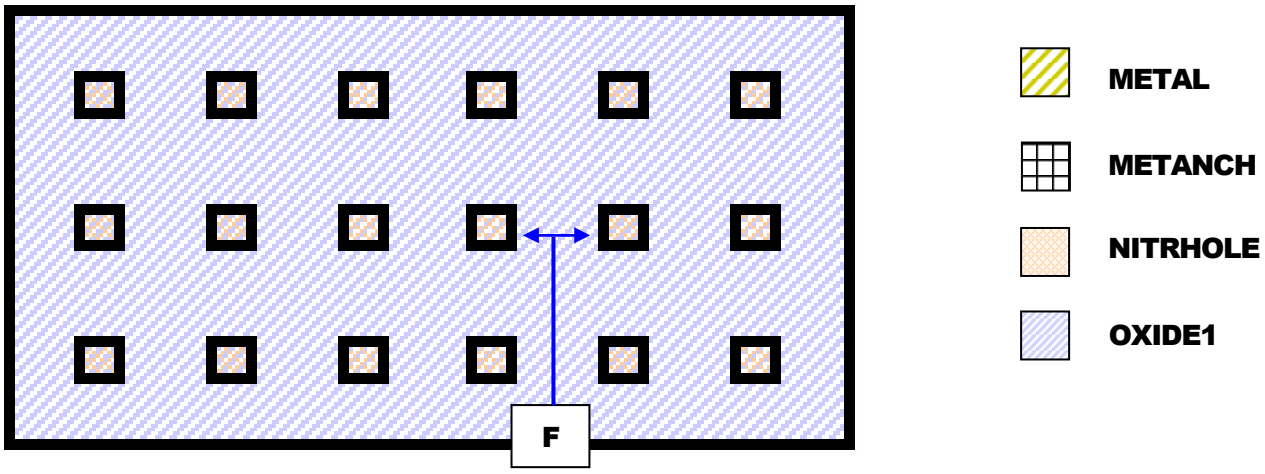
FIGURE 2.3.7

A: OXIDE1 enclose NITRHOLE > 5.0µm. The amount that Oxide 1 must extend beyond the edge of NITRHOLE to ensure proper trench formation

C: NITRHOLE space to POLY > 5.0µm. The spacing between NITRHOLE and a Poly edge to ensure protection of the poly during the KOH trench etching

E: METAL enclose METANCH > 5.0µm. The amount that Metal must extend beyond the edge of METANCH to ensure complete coverage of the hole.

Perforated Nitride Membrane Over Trench



Perforated Metal (Nickel) Membrane Over Trench

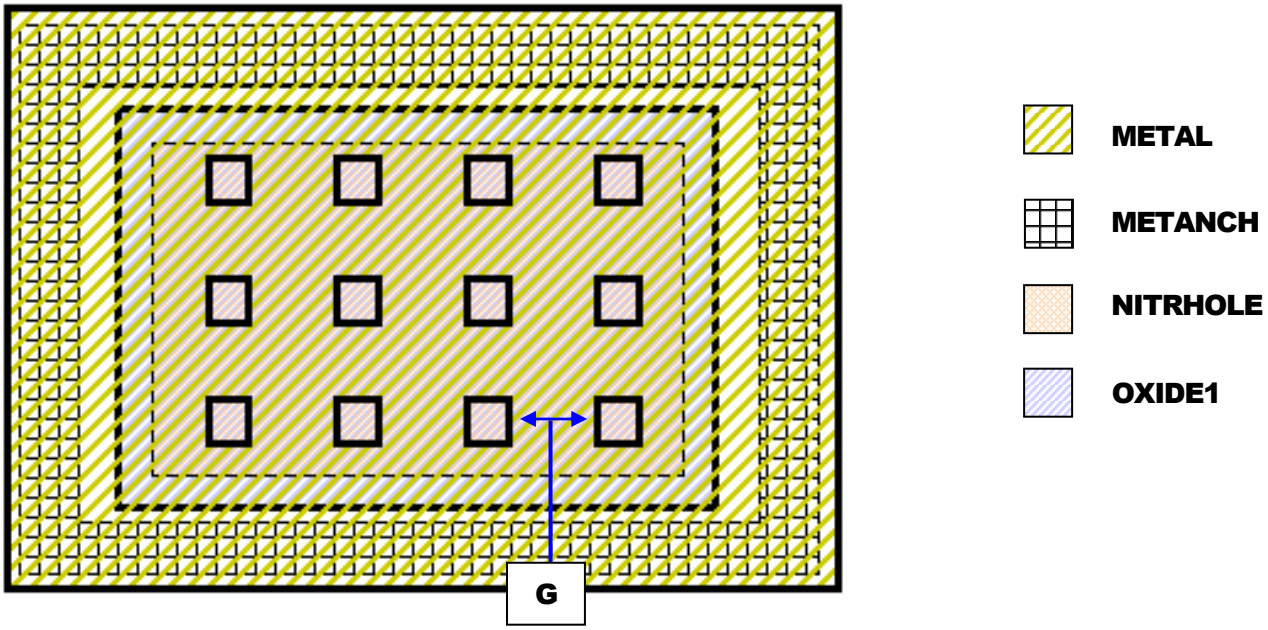


FIGURE 2.3.8

F: Lateral Etch Holes Space In Nitride <100µm. Minimum spacing between holes in Nitride to ensure that the Nitride structure is completely released and the trench is formed properly.

G: Lateral Etch Holes Space In Metal <100µm. Minimum spacing between holes in Metal to ensure that the Metal structure is completely released.

2.3.3. Designs Rules for the GOLDOVP Level

The GOLDOVP layer is an optional masking and process layer in the MetalMUMPs process. The original intent of this layer was to provide a low contact resistance material (Gold) along the sidewalls of plated Nickel structures that would make electrical contact when a microrelay structure was actuated to a closed switch position.

Table 2.5 lists the design rules associated the GOLDOVP level. The rules are given in each line of the table along with a figure number and a rule letter. Figure 2.3.9 is a plan view that illustrates the GOLDOVP rules.

Rule	Rule Letter	Figure #	Min. Value (μm)
GOLDOVP enclose METAL	H	2.3.9	10.0
GOLDOVP space to METAL	I	2.3.9	10.0
GOLDOVP space to METANCH	J	2.3.9	50.0

TABLE 2.5. Design Rules for the Optional GOLDOVP Level

Rule H defines proper enclosure of a Metal feature to ensure that the sidewall of the Metal feature is over plated with gold.

Rule I defines the minimum spacing between a GOLDOVP opening edge and a Metal feature edge to ensure that the Metal feature is *not* over plated with gold.

Rule J defines the minimum spacing between a GOLDOVP opening edge and a METANCH opening edge to ensure that the metal anchor is not compromised during the removal of the plating base metal.

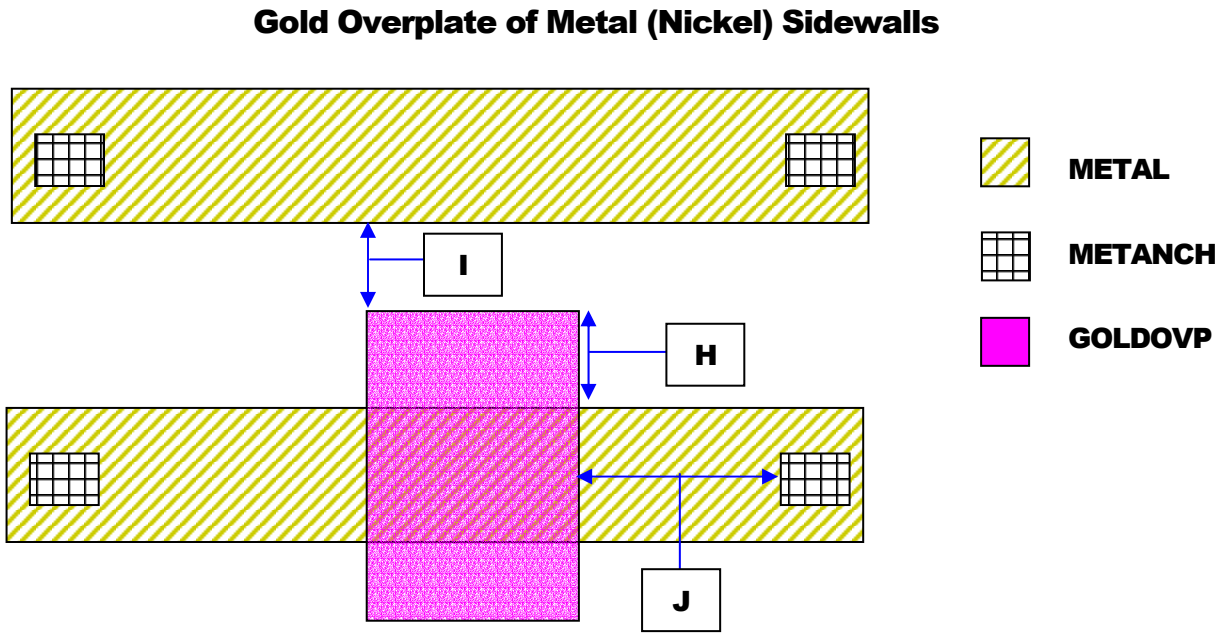


FIGURE 2.3.9

H: GOLDOVP enclose METAL > 10µm. The amount that the GOLDOVP opening must extend beyond the edge of METAL to ensure over plating of the sidewall of the Metal feature.

I: GOLDOVP space to METAL > 10µm. The spacing between GOLDOVP and a Metal edge to ensure sidewall of the Metal feature does not get overplated.

J: GOLDOVP space to METANCH > 50µm. The spacing between GOLDOVP and a METANCH edge to ensure protection of the Metal anchor.

2.3.4. Summary

Table 2.6 summarizes the MetalMUMPs design rules.

Level 1	Level 2	Min. Feature	Min. Spacing	Enclose/ Rule	Spacing/ Rule
OXIDE1	-	20	20		
	NITRHOLE			5.0 / A	
POLY	-	5	5		
	NITRHOLE			5.0 / B	
NITRHOLE	-	5	5		
	POLY				5.0 / C
METANCH	-	50	10		
METAL	-	8	8		
	NITRHOLE			25.0 / D	
	METANCH			5.0 / E	
GOLDOVP	-	50	50		
	METAL			10.0 / H	10.0 / I
	METANCH				50.0 / J
HOLEM		5	5		
HOLEP		8	8		

TABLE 2.6. Design rule reference sheet. Table shows minimum dimensions (µm) and rule name.

2.4. Beyond the Design Rules

Section 2.4 is highly recommended reading for any MetalMUMPs user, novice or experienced. It includes information that will optimize your MetalMUMPs design for success, and should prevent several common design errors.

2.4.1. Layout convention

The following convention used by the METALMUMPs processes in defining mask levels: For the OXIDE1, POLY, and METAL levels the masks are light field. For these levels, draw (i.e. digitize) the feature you want to keep. The NITRHOLE, METANCH, GOLDOVP, HOLEP and HOLEM levels are dark field. For these levels, draw the hole you want to make. It is imperative that these conventions be followed for your devices to be fabricated correctly.

2.4.2. Electroplated metal uniformity

The thickness and uniformity of the electroplated nickel (Metal) is strongly dependent upon the area of die that is covered with Metal. In order to minimize non-uniformities, and to ensure that the pattern from one chip design does not influence the Metal thickness and uniformity of a neighboring chip design, we require that the area of plated Metal be constrained as follows:

- **30% of Chip Area < Area of plated Metal < 40% of Chip Area**

That is, the total area of plated Metal should be between 30% and 40% of the total chip area.

When laying out devices on a chip, it is best to uniformly distribute the Metal structures. Open areas should be filled with "dummy" structures, if necessary. **THIS IS A MANDATORY RULE**.

2.4.3. Enclosing Adjacent Lines of Poly in Nitride

Enclosing adjacent lines of Poly (e.g., a serpentine resistor pattern) in Nitride is best done with a single "sheet" of nitride as opposed to a "broken" patterned nitride layer. The single sheet of nitride offers better mechanical stability and protection for the Poly layer during the KOH trench etch.

2.4.4. Removing Nitride from the "Field" Regions

Removing the Nitride layers from the "Field" regions of the chip should be avoided.

2.4.5. Release and Trench Etch Rules

- Anywhere there is a NITRHOLE that is not over Poly, a trench in the silicon substrate will be formed unless this area is covered with METAL

- All NITRHOLE over Poly must have METAL with at least the minimum overlap. Failure to adhere to this rule will result in attack of the polysilcon during the KOH trench etch.

- Oxide 1 must be present (OXIDE1 mask layer) wherever it is desired to release nitride (Nitride 1 and Nitride 2).

- Trenches are formed with a KOH silicon etch process. This type of etching is anisotropic in that the <111> crystal plane etches much slower than the other planes. For the silicon substrate that is used in this process the <111> planes are parallel to the edges of the die and sloped at an angle of 54.7^{o} with respect to the wafer surface. Trenches that are not along these planes or have convex corners will result in

significant undercut of the Nitride layer which can result in cracking and breaking off of the over-hanging Nitride. For more information on anisotropic wet etching of silicon refer to Madou[1], Chapter 4.

2.4.6. Design Hints to Maintain Nitride Integrity During Release (Temporary Anchors)

Our experience has shown that anchoring Metal (nickel) to released Nitride structures can result in cracking of the nitride and attack of underlying polysilicon if proper design guidelines are not employed. This potential cracking is due to temporary stress imbalance conditions experienced during the release. To minimize this stress imbalance, it is best to release the nitride structure during the trench etch rather than during the Oxide release etch. "Temporary Anchors" are fabricated by removing Oxide 1 in strategic areas under the nitride membrane such that the HF release etch will not undercut it enough to release it, but it will be undercut during the KOH trench etch. Figure 2.4.1 provides an example of a design utilizing "temporary anchors" that will eliminate or minimize the potential for Nitride cracking during the release.

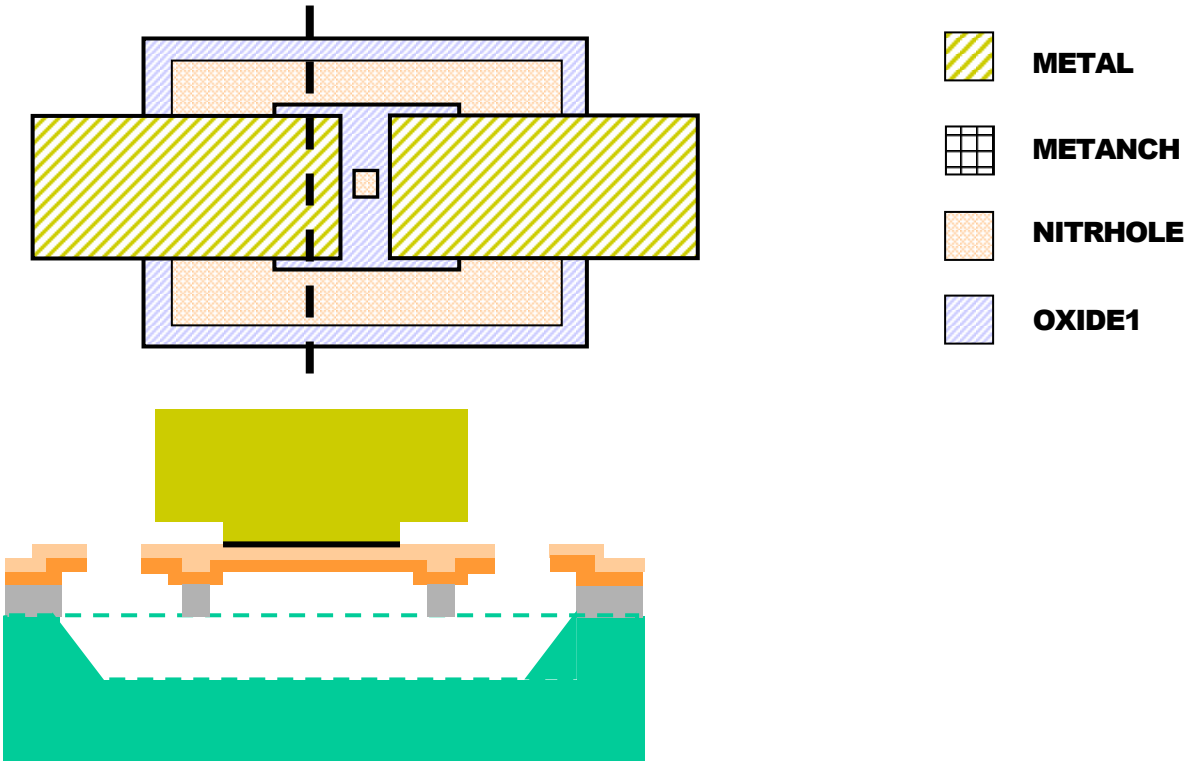


FIGURE 2.4.1 Example of Temporary Anchor use: Holes in Oxide 2 prevent the Nitride/Metal structure from being released during the HF release etch. The structure is released during the KOH trench etch instead. Note that some Isolation Oxide may remain on the bottom side of the Nitride.

	Substrate		Oxide 1		Poly		Oxide 2		Metal
	Isolation Oxide		Nitride 1		Nitride 2		Anchor Metal		Sidewall Metal
	Photoresist								

[1] Madou, Mark (1997). Fundamentals of Microfabrication. Boca Raton, Florida: CRC Press, LLC.

2.4.7. Gold overplate, enclosing of entire structures

If an entire Metal structure is enclosed with the GOLDOVP level, no gold will be deposited on the sidewalls of the structure. The plating base provides the necessary electrical contact for the gold plating process. Prior to the gold plating process, the plating base is removed from the area inside the GOLDOVP hole. If the Metal to be overplated is completely enclosed, the structure will be electrically isolated from the rest of the metal, and will not be gold plated. Refer to figure 2.4.2 for an example.

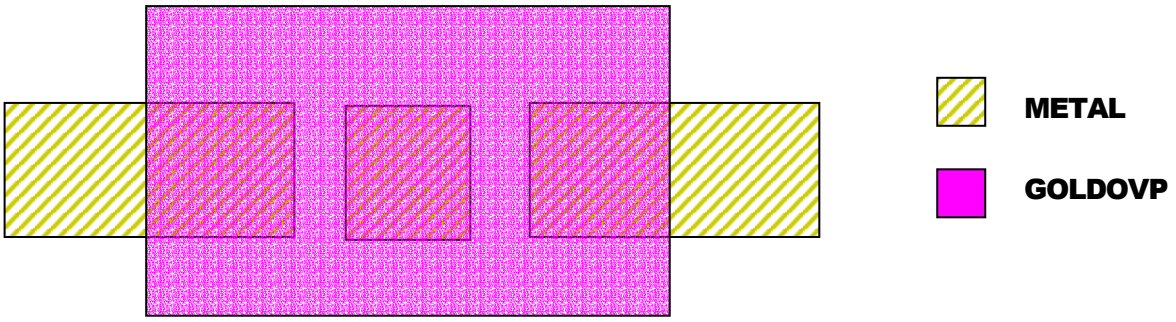


FIGURE 2.4.2: Metal structure in center will be electrically isolated from the rest of the wafer and will NOT be gold overplated.

2.4.8. Labeling of designs on die:

Labeling of structures/die must follow the design rules in order to ensure that they will be legible and remain intact during the release processes. Labels can be formed with Poly, Anchor Metal, or Metal. All Oxide must be removed under labels. Metal labels should be properly anchored to the substrate (Isolation Oxide). Poly labels should be completely covered with Nitride with appropriate overlaps as defined by the design rules. For Metal labels, using holes in a large block of Metal is a good practice to ensure that the label will remain throughout the process as shown in figure 2.4.3. Alternatively, the metal label could be attached to another large Metal structure.

FIGURE 2.4.3 Creating Labels with METAL level: a) Best practice. This label design will minimize the size required to ensure that it remains throughout the process. b) For this label to remain intact throughout the process, all of the letters must have minimum line widths >50μm.

2.5. Film Parameters

The thickness, stress, and resistivity of relevant layers in the MetalMUMPs process are summarized in Table 2.6. This data is based on measurements from previous runs.

Film	Thickness (nm)			Residual Stress (MPa)			Resistance (ohm/sq)		
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
Isolation Oxide	1900	2000	2100	N/A			N/A		
Oxide 1	450	500	550	N/A			N/A		
Nitride 1	315	350	365	0	90	180	N/A		
Poly 1	630	700	770	N/A			19	22	25
Nitride 2	315	350	365	0	90	180	N/A		
Oxide 2	990	1100	1210	N/A			N/A		
Anchor Metal	32	35	38	N/A			--	7	--
Plating Base	495	550	605	N/A			N/A		
Metal	17000	20000	23000	--	100	--	--	8 μohm*cm	--
Sidewall Metal	1000	2000	3000	N/A			N/A		
Trench	N/A	25000	N/A	N/A			N/A		

TABLE 2.6. Mechanical and electrical parameters of MetalMUMPs process layers.

2.6. Layout Requirements

2.6.1. Usable Area

The maximum allowed design area for MetalMUMPs is 1 cm x 1 cm. Care should be taken to avoid placing structures closer than 100μm from the edge of the die since dicing can occasionally damage the edge of the chip.

2.6.2. Cell Name Restrictions

Some errors have occurred in the past due to nonstandard cell names. In order to reduce these errors and the time it takes to translate designs, some guidelines need to be put in place. They are as follows:

1). Cell names should be under 28 characters.

2). Cell names should consist of only the following characters or numerals [a-zA-Z0-9] and the underscore character '_'.

2.6.3. Layer Names

Layouts must use layer names as indicated in Table 2.3. For CIF submissions the indicated names should be used (i.e. for NITRHOLE use NITR) and for GDS submissions the correct number must be used. Other layers may be in the design; but they will be ignored. MEMSCAP is not responsible for layers omitted due to failure to comply with naming conventions.

2.6.4. General Layout Tips and Known Software Bugs

The software currently used to assemble the MetalMUMPs masks does a reasonable job with most translations; however, there are some additional nuances of which users should be aware**.**

Keep in mind that these are the bugs that MEMSCAP is aware of - we are not responsible for problems resulting from other bugs not listed here.

1). In GDS, three wire types are allowed, extended, butted, and rounded ends. Rounded ended wires will be converted to an octagon ending. It is strongly suggested that only extended wire types be used with CIF files; otherwise, information may be lost and connections broken.

2). L-Edit versions 7 and 8, up until version 8.22, have a bug. The bug comes from the donut command in L-Edit which becomes a filled circle when written out to gds and translated into other programs. If you use a donut, be sure to use the horizontal or vertical cut commands to break the donut into multiple polygons.

3). There is a bug in L-Edit versions before 8.41 when working with rotated and mirrored instances. If an instance is rotated and mirrored, then saved to gds, the rotation angle will be rounded off to the nearest degree (i.e. An instance is rotated 22.2 degrees and then mirrored, after saving to gds and reading back in, the angle will be changed to 22 degrees.

Fix: The cell referencing this instance should be flattened.

4). The software will create an error if an illegal polygon is produced during translation. Figure 2.6.1 illustrates an example of this problem. Most layout tools deal with this polygon correctly. To fix the problem the points can be made common or the polygons resized slightly. If there are a relatively small number of errors, MEMSCAP will make the modifications. However if that number is large, the user may be requested to make the changes. The types of errors very often occur in lettering and in pictures that have been translated to gds.

FIGURE 2.6.1 An Illegal polygon (left) and a correct polygon(right) are shown.

5) Translations of polygons with numbers of vertices over 1000 can also be translated incorrectly. These often come from mechanical drawings and should be broken down into smaller polygons before submission.

2.6.5. Design Rule Checking

PLEASE NOTE THAT NO ERROR CHECKING WILL BE DONE ON YOUR DESIGN. We have versions of DRC files for Tanner, Cadence, and Mentor software. To get these, send an email to *mems@memsrus.com.*

2.7. Layout Submission

Designs may be submitted in GDSII™ **(preferred)** or CIF formats only. Technology files for L-Edit™, Cadence™, Magic™ and Mentor's layout tool may be requested via email at *mems@memsrus.com.*

Before submitting your design, you must complete the Design Submission Form on our website at *http://www.memsrus.com/cronos/svcsdes.html.* Once we have received your completed form, you will receive an email with instructions and access information to upload your file to our ftp site.