MEMS-specific fabrication

- Bulk micromachining
- Surface micromachining
- Deep reactive ion etching (DRIE)
- Other materials/processes

Bulk, Surface, DRIE

- Bulk micromachining involves removing material from the silicon wafer itself
  - Typically wet etched
  - Traditional MEMS industry
  - Artistic design, inexpensive equipment
  - Issues with IC compatibility
- Surface micromachining leaves the wafer untouched, but adds/removes additional layers above the wafer surface, First widely used in 1990s
  - Typically plasma etched
  - IC-like design philosophy, relatively expensive equipment
  - Different issues with IC compatibility
- Deep Reactive Ion Etch (DRIE) removes substrate but looks like surface micromachining!

Bulk Micromachining

- Many liquid etchants demonstrate dramatic etch rate differences in different crystal directions
  - <111> etch rate is slowest, <100> and <110> fastest
  - Fastest:slowest can be more than 400:1
  - KOH, EDP, TMAH most common anisotropic silicon etchants
- Isotropic silicon etchants
  - HNA
    - HF, nitric, and acetic acids
    - Lots of neat features, tough to work with
  - XeF_2, BrF_3
    - gas phase, gentle
    - Xactix, STS selling research & production equipment

KOH Etching

- Etches PR and Aluminum instantly
- Masks:
  - SiO2
    - compressive
  - SixNy
    - tensile
  - Parylene!
  - Au?

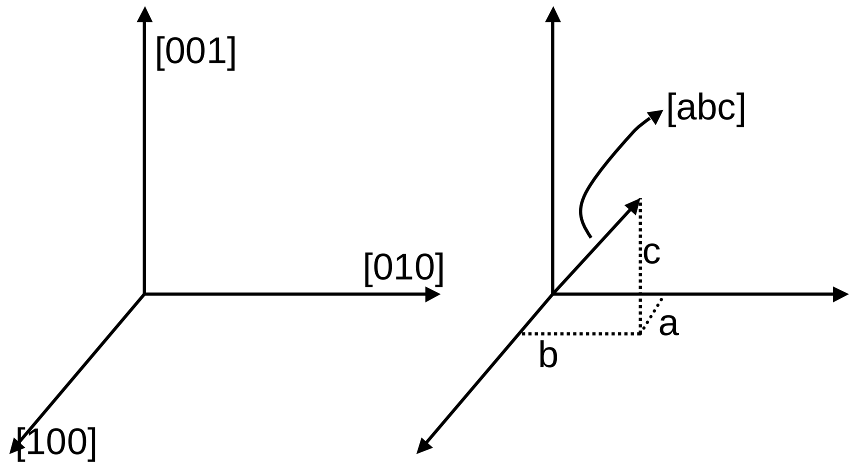
Crystal Planes & Miller Indices

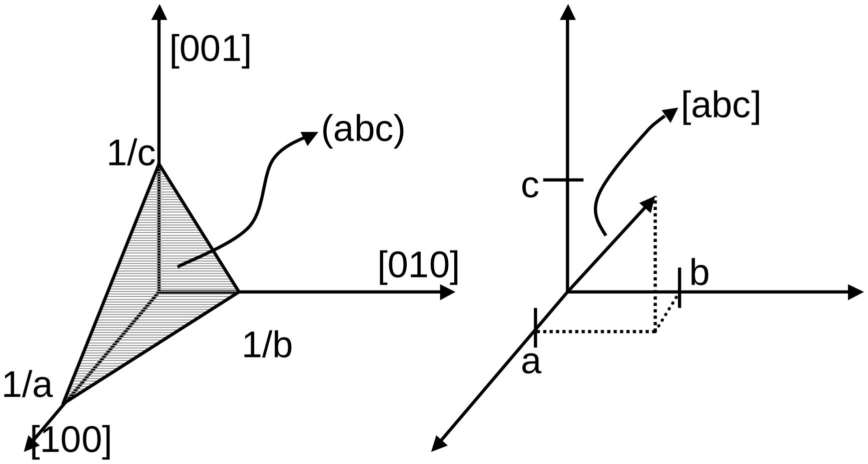
- [abc] in a cubic crystal is just a direction vector
- (abc) is any plane perpendicular to the [abc] vector
- (…)/[…] indicate a specific plane/direction
- {…}/<…> indicate equivalent planes/direction

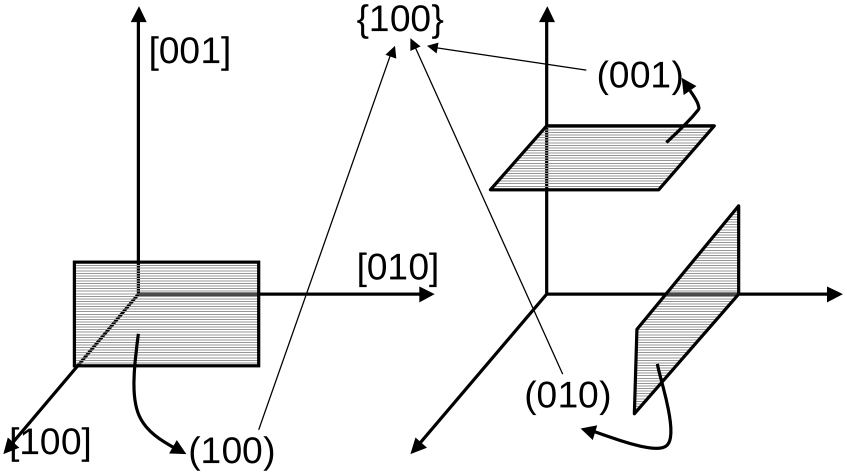
Angles between directions can be determined by scalar product: the angle between [abc] and [xyz] is given by ax+by+cz = |(a,b,c)|*|(x,y,z)|*cos(theta)

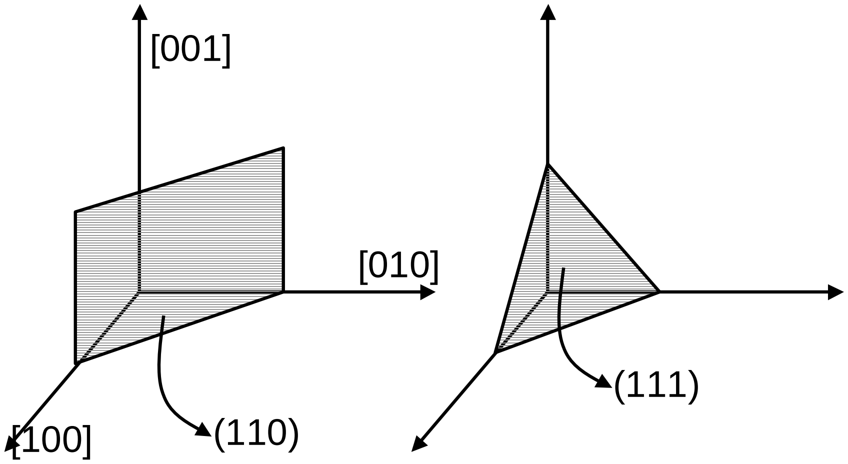
e.g.: $\theta_{(100),(111)} = Cos^{-1}((1+0+0)/(1)(\sqrt{3}))$

Miller indices

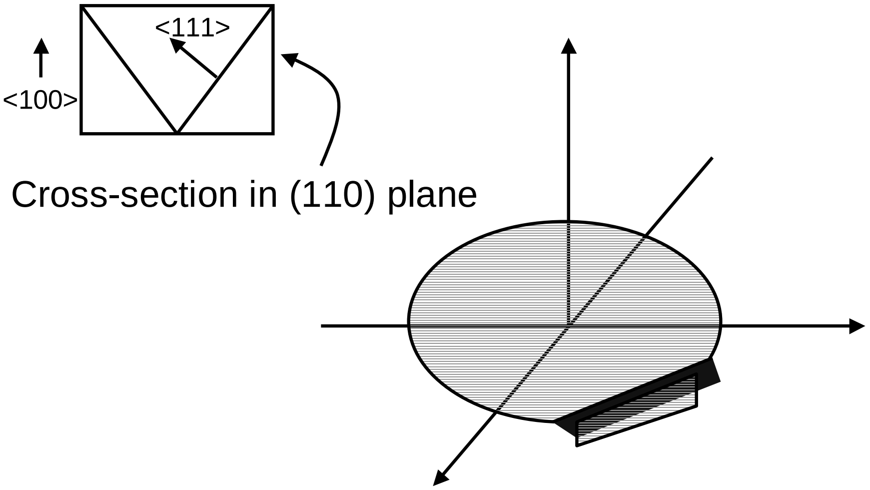



[001]
(abc)
1/c
[010]
1/b
1/a
[100]
[abc]
c
b
a


{100}
[001]
(001)
[010]
(010)
[100]
(100)

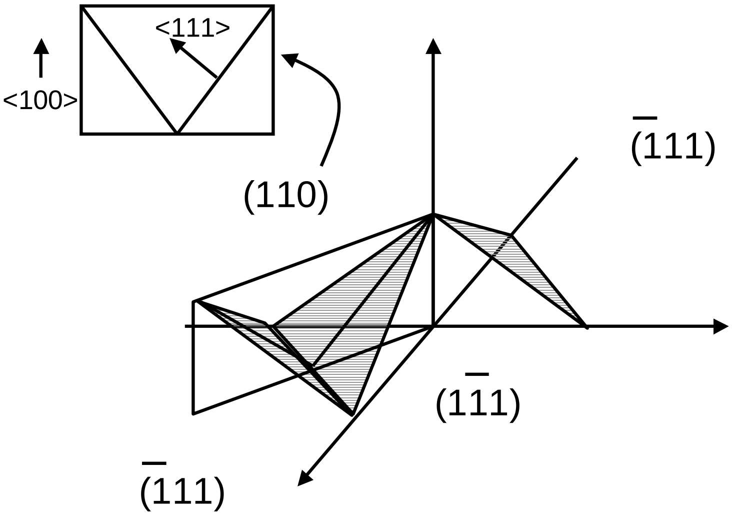


Typical 100 wafer

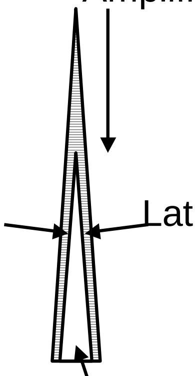


Cross-section in (110) plane

The wafer flat is oriented in the [110] direction



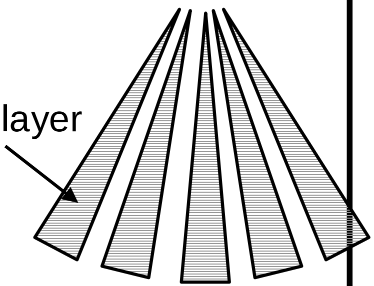
Rosette



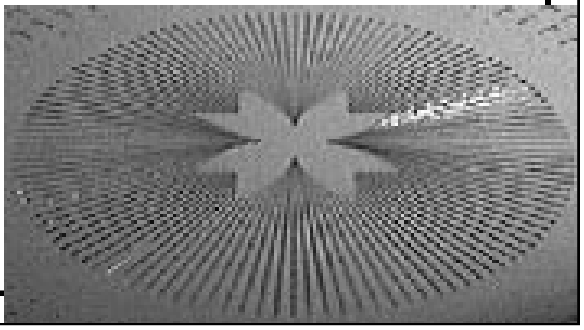
"Amplified" etch rate

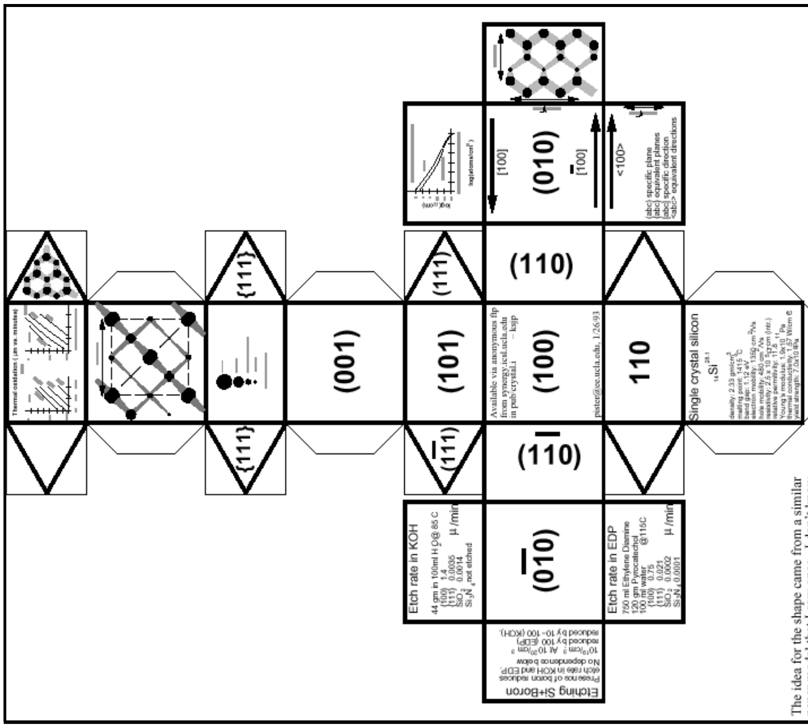
Lateral undercut

Un-etched silicon



Masking layer





The idea for the shape came from a similar paper model that I saw once. I don't know who made that one. Perhaps Monsanto?
Most of the data comes from "Silicon as a mechanical Material", by Peterson (Proc.IEEE, v70n5, 1982, pp.420–457).
Other data from "VLSI Technology", edited by Sze (McGraw–Hill) and "Solid State Electronic Devices", by Streetman (Prentice–Hall).

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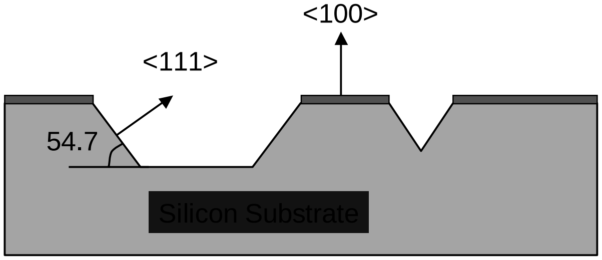
Anisotropic Etching of Silicon



- Anisotropic etches have direction dependent etch rates in crystals
- Typically the etch rates are slower perpendicularly to the crystalline planes with the highest density
- Commonly used anisotropic etches in silicon include Potasium Hydroxide (KOH), Tetramethyl Ammonium Hydroxide (TmAH), and Ethylene Diamine Pyrochatecol (EDP)

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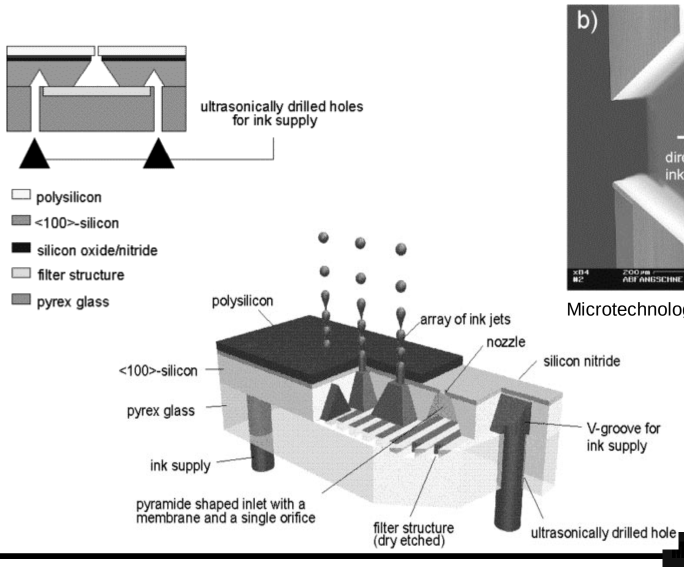
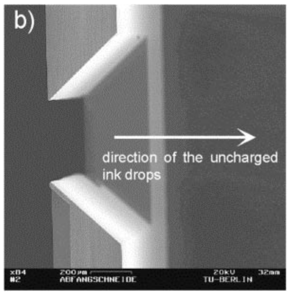
Etch stops in anisotropic silicon etching

- Electrochemical etch stop
- High boron doping (~1e20/cm)

Micromachining Ink Jet Nozzles

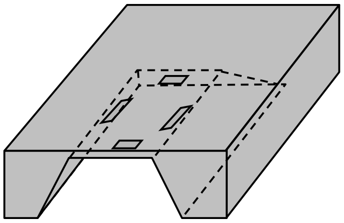




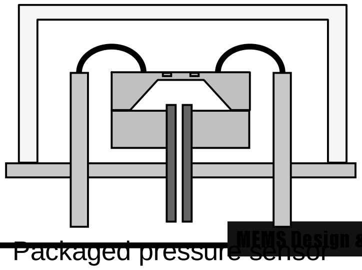
Microtechnology group, TU Berlin

Bulk Micromachining

- Anisotropic etching allows very precise machining of silicon
- Silicon also exhibit a strong piezoresistive effect
- These properties, combined with silicon’s exceptional mechanical characteristics, and well-developed manufacturing base, make silicon the ideal material for precision sensors
- Pressure sensors and accelerometers were the first to be developed

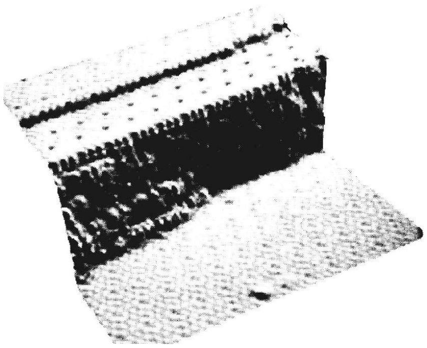


Silicon pressure sensor chip



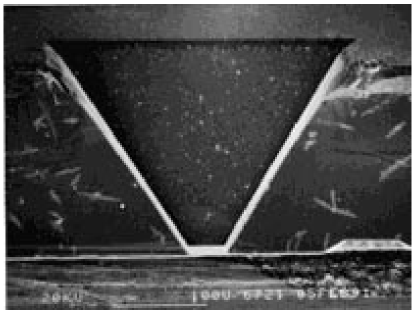
Packaged pressure sensor

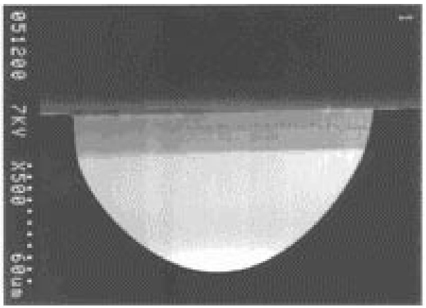
KOH etching: atomic view



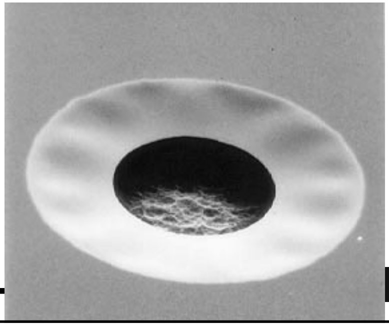
STM image of a (111) face with a ~10 atom step. From Weisendanger, et al., *Scanning tunnelling microscopy study of Si(111)7*7 in the presence of multiple-step edges*, Europhysics Letters, 12, 57 (1990).

Bulk micromachined cavities





- Anisotropic KOH etch (Upperleft)
- Isotropic plasma etch (upper right)
- Isotropic BrF3 etch with compressive oxide still showing (lower right)



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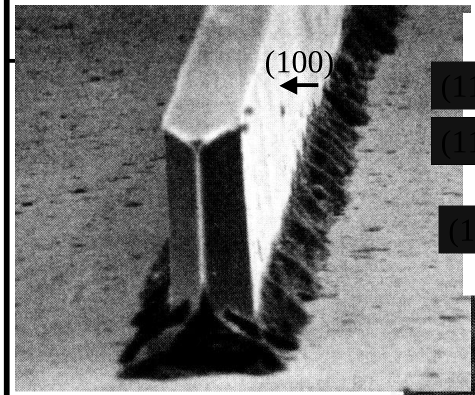
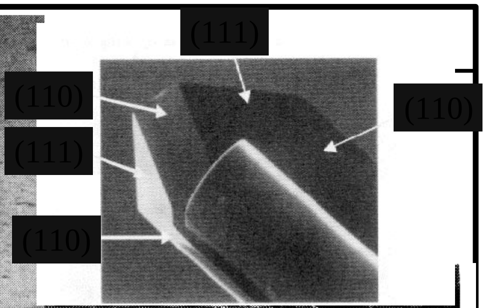
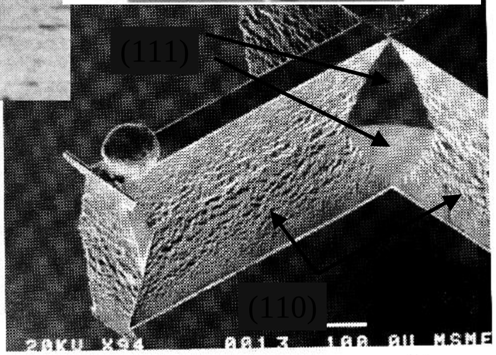




Clever KOH etching of (100)

Clockwise from above: Ternez; Rosengren; Keller



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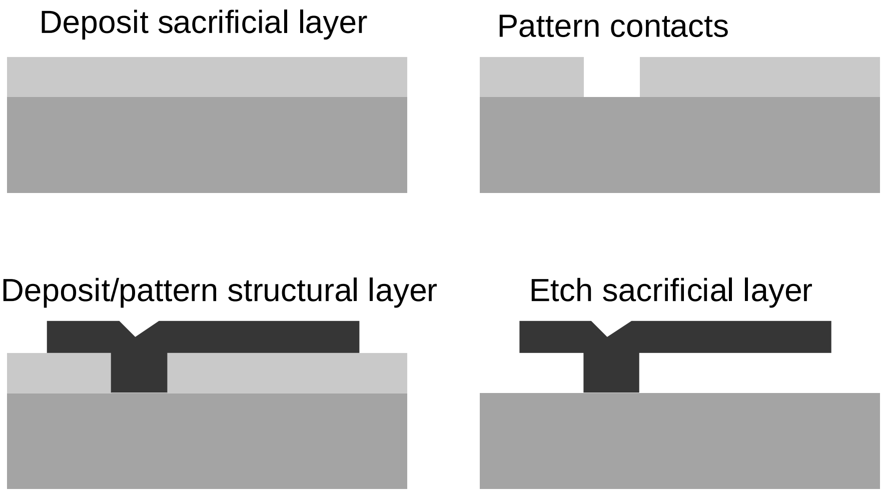
Surface Micromachining


Deposit sacrificial layer

Pattern contacts

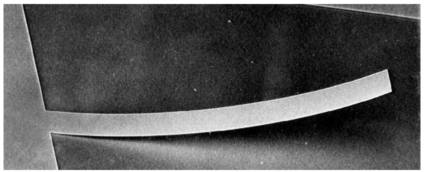
Deposit/pattern structural layer

Etch sacrificial layer

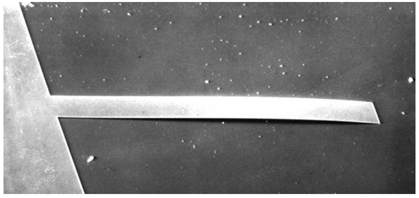
Surface micromachining material systems

Structure/	sacrificial/	etchant
Polysilicon/	Silicon dioxide/	HF
Silicon dioxide/	polysilicon/	XeF2
Aluminum/	photoresist/	oxygen plasma
Photoresist/	aluminum/	Al etch
Aluminum/	SCS	EDP, TMAH, XeF2
Poly-SiGe	poly-SiGe	DI water

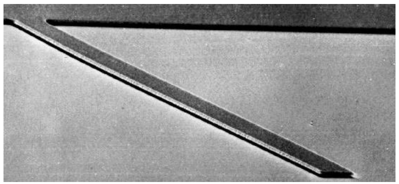
Residual stress gradients



More tensile on top

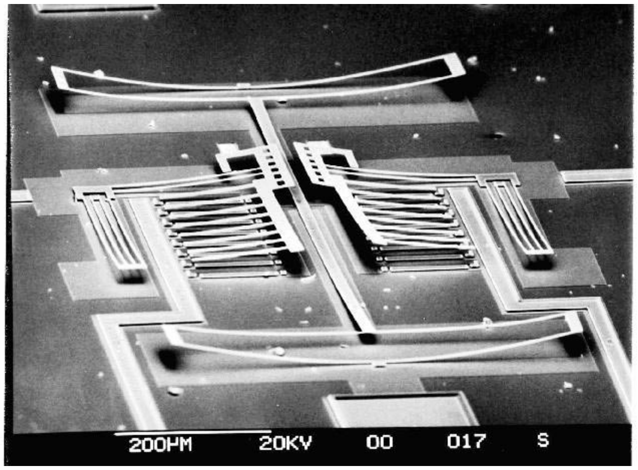


More compressive on top



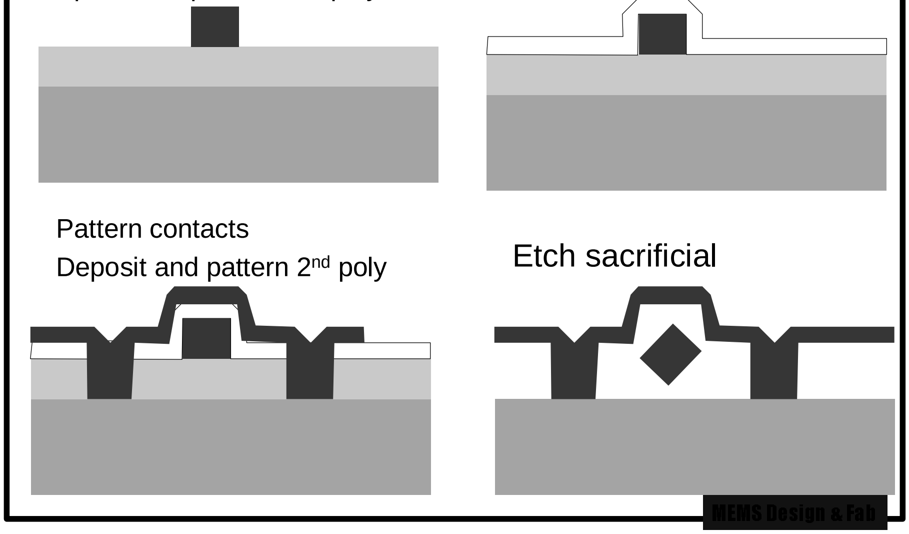
Just right! The bottom line: anneal poly between oxides with similar phosphorous content. ~1000C for ~60 seconds is enough.

Residual stress gradients



A bad day at MCNC (1996).

Hinges



Deposit first sacrificial

Deposit and pattern first poly

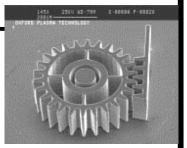
Deposit and pattern second sacrificial

Pattern contacts

Deposit and pattern 2nd poly

Etch sacrificial

Deep Reactive Ion Etch

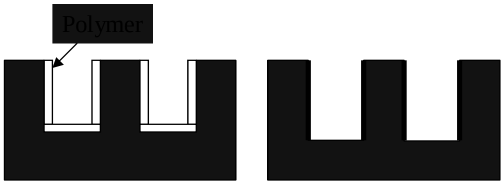


BOSCH Patent STS, Alcatel, Trion, Oxford Instruments …

Uses high density plasma to alternatively etch silicon and deposit a etch-resistant polymer on side walls

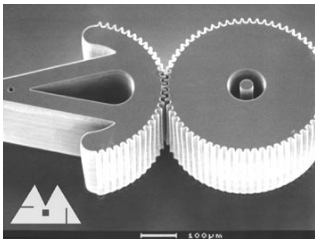
☺
- Unconstrained geometry
- 90° side walls
- High aspect ratio 1:30
- Easily masked (PR, SiO2)

☹ Process recipe depends on geometry

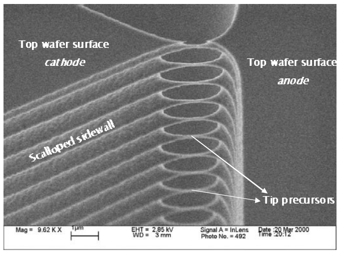


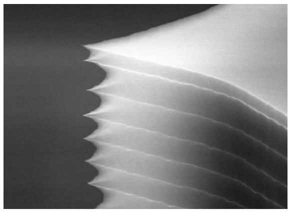
Polymer deposition

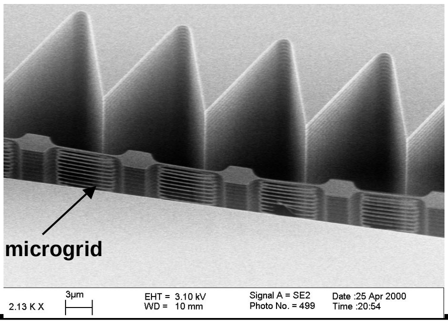
Silicon etch using SF_6 chemistry

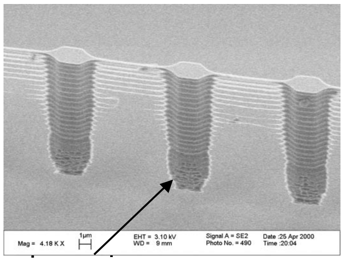


Scalloping and Footing issues of DRIE







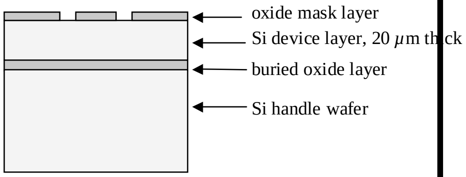


Footing at the bottom of device layer

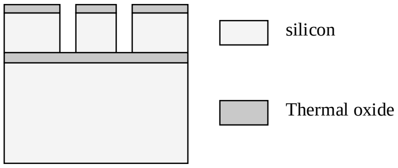
Milanovic et al, IEEE TED, Jan. 2001.

Typical simple SOI-MEMS Process

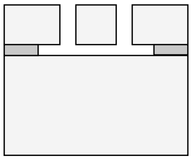
1) Begin with a bonded SOI wafer. Grow and etch a thin thermal oxide layer to act as a mask for the silicon etch.



2) Etch the silicon device layer to expose the buried oxide layer.

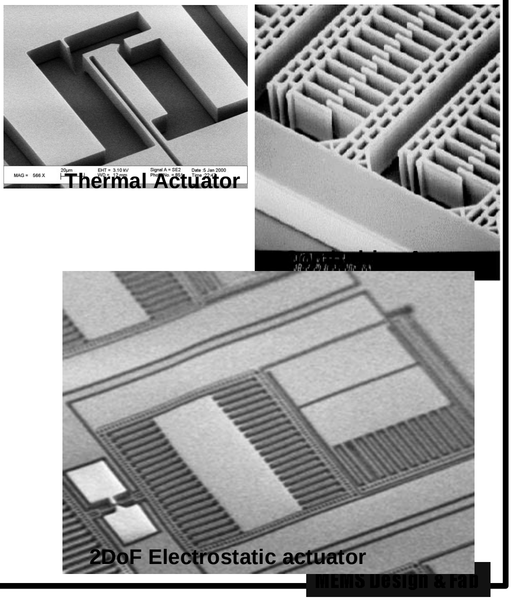


3) Etch the buried oxide layer in buffered HF to release free-standing structures.



DRIE structures

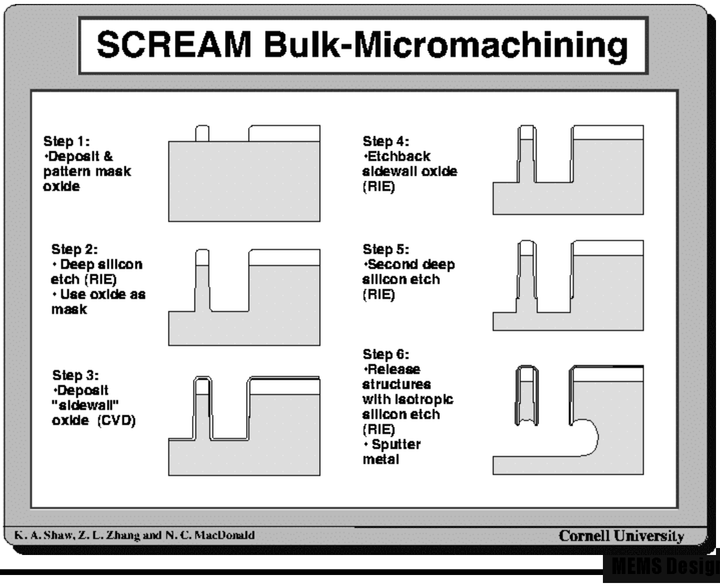
- Increased capacitance for actuation and sensing
- Low-stress structures
  - single-crystal Si only structural material
- Highly stiff in vertical direction
  - isolation of motion to wafer plane
  - flat, robust structures



Thermal Actuator

2DoF Electrostatic actuator

SCREAM fab flow



SCREAM Bulk-Micromachining

Step 1:
·Deposit & pattern mask oxide

Step 2:
· Deep silicon etch (RIE)
· Use oxide as mask

Step 3:
·Deposit "sidewall" oxide (CVD)

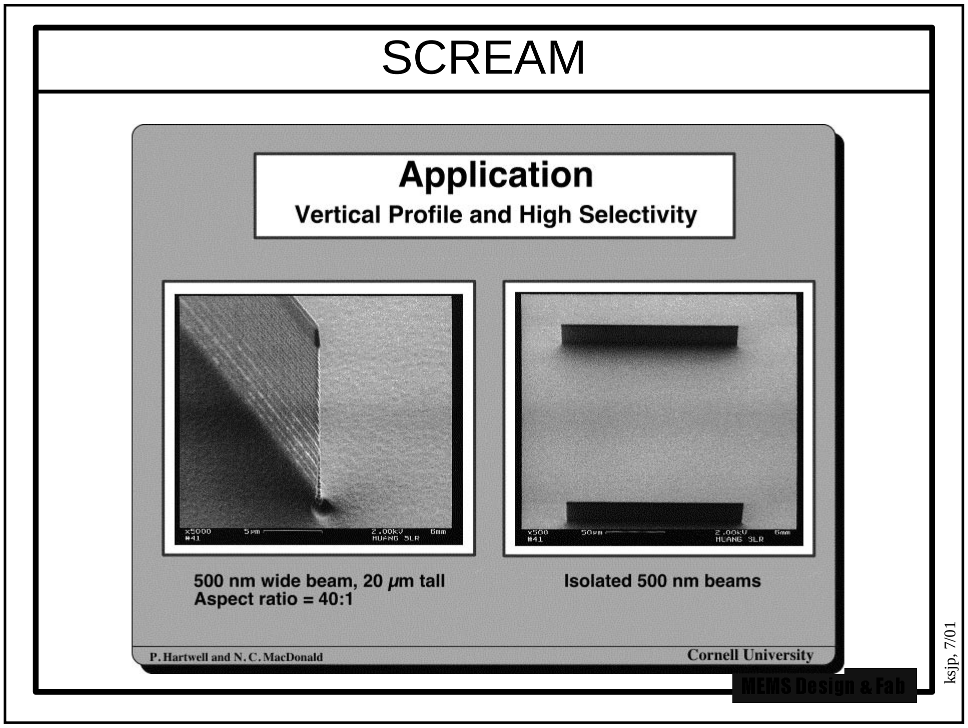
Step 4:
·Etchback sidewall oxide (RIE)

Step 5:
·Second deep silicon etch (RIE)

Step 6:
·Release structures with isotropic silicon etch (RIE)
· Sputter metal

K. A. Shaw, Z. L. Zhang and N. C. MacDonald

Cornell University



SCREAM

Application

Vertical Profile and High Selectivity

500 nm wide beam, 20 μm tall
Aspect ratio = 40:1

Isolated 500 nm beams

P. Hartwell and N. C. MacDonald

Cornell University

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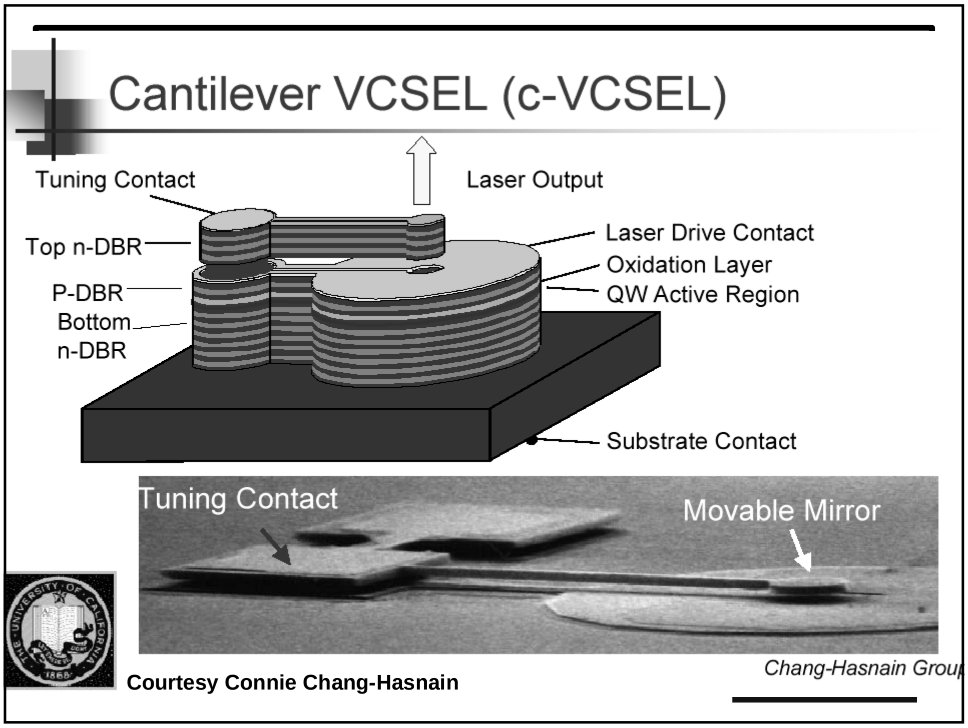
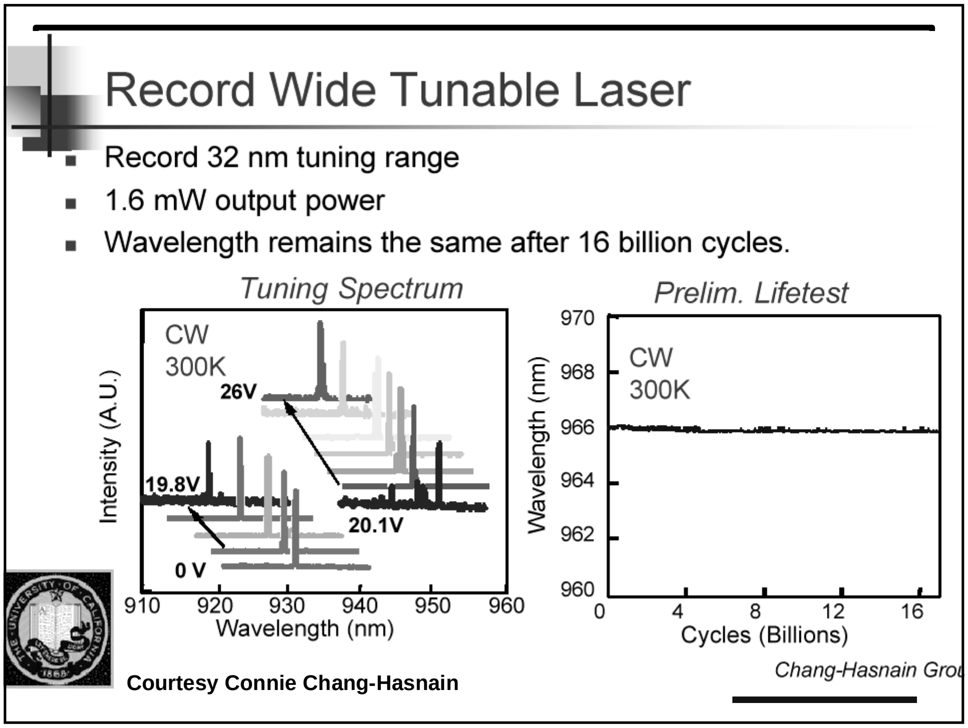


Cantilever VCSEL (c-VCSEL)

Courtesy Connie Chang-Hasnain

Chang-Hasnain Grou

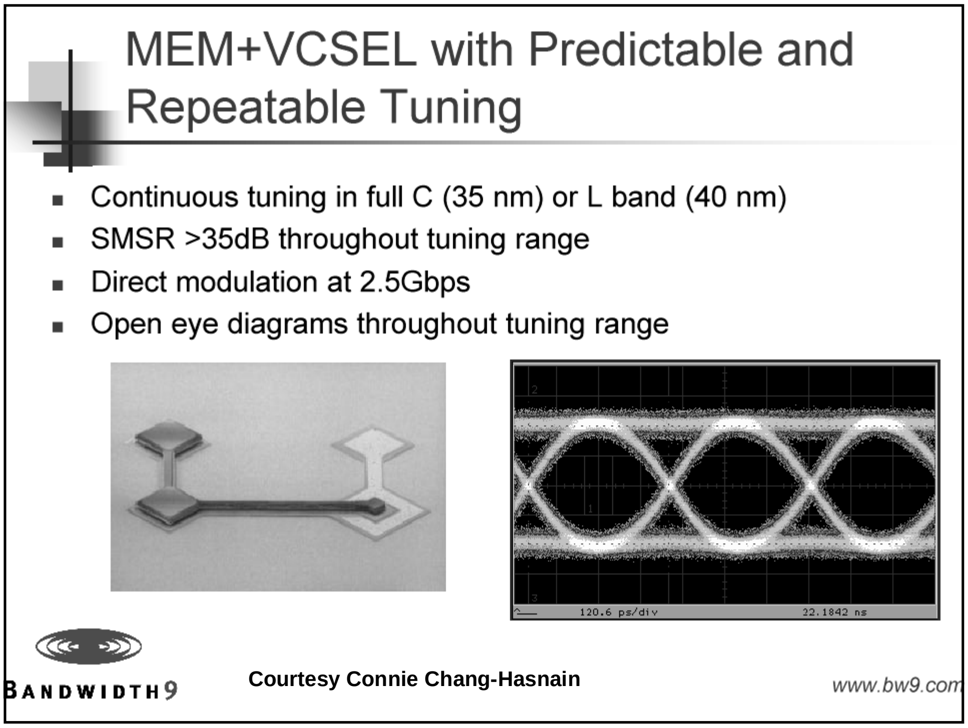


Record Wide Tunable Laser

- Record 32 nm tuning range
- 1.6 mW output power
- Wavelength remains the same after 16 billion cycles.

Courtesy Connie Chang-Hasnain

Chang-Hasnain Gro



MEM+VCSEL with Predictable and Repeatable Tuning

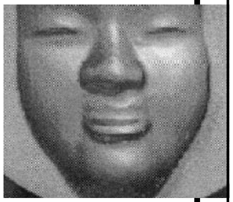
- Continuous tuning in full C (35 nm) or L band (40 nm)
- SMSR >35dB throughout tuning range
- Direct modulation at 2.5Gbps
- Open eye diagrams throughout tuning range

Courtesy Connie Chang-Hasnain

www.bw9.com

ULTRA-PRECISION MICRO STRUCTURING BY MEANS OF MECHANICAL MACHINING

Tomohiko Kawai*, Kiyoshi Sawada*, and Yoshimi Takeuchi**
* FANUC Ltd., 3580 , Shibokusa , Oshino , Yamanashi 401-0597 , Japan
E-mail : sawada.kiyoshi@fanuc.co.jp



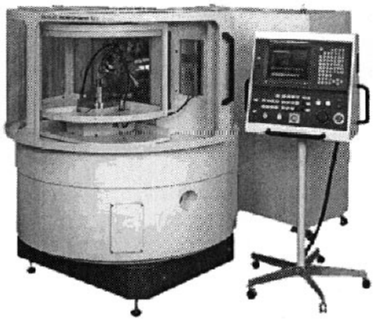
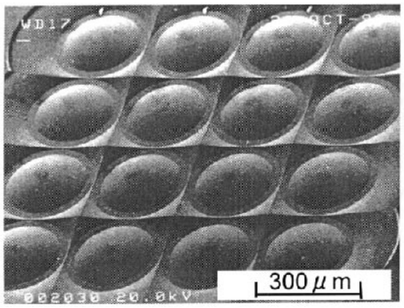


Figure 1. Whole xiew of FANUC ROBOnano Ui



Sub-Micron Stereo Lithography

New Micro Stereo Lithography for Freely Movable 3D Micro Structure
-Super IH Process with Submicron Resolution-

Koji Ikuta, Shoji Maruo, and Syunsuke Kojima
Department of Micro System Engineering, school of Engineering, Nagoya University
Furocho, Chikusa-ku, Nagonya 464-01, Japan
Tel: +81 52 789 5024, Fax: +81 52 789 5027 E-mail: ikuta@mech.nagoya-u.ac.jp

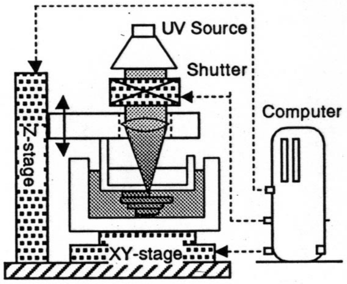


Fig. 1 Schematic diagram of IH Process

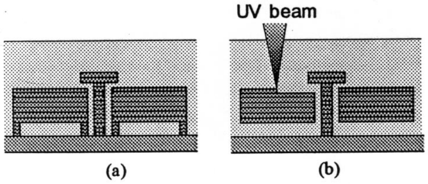


Fig. 5 Process to make movable gear and shaft
(a) conventional micro stereo lithography needs base layer
(b) new super IH process needs no base

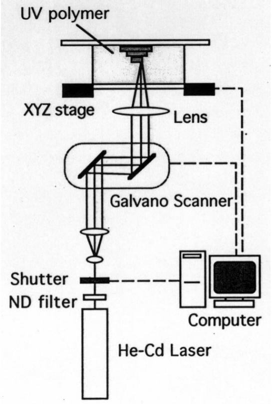


Fig. 6 Schematic diagram of the super IH process

Micro Electro Mechanical Systems
Jan., 1998 Heidelberg, Germany

Sub-Micron Stereo Lithography

New Micro Stereo Lithography for Freely Movable 3D Micro Structure

-Super IH Process with Submicron Resolution-

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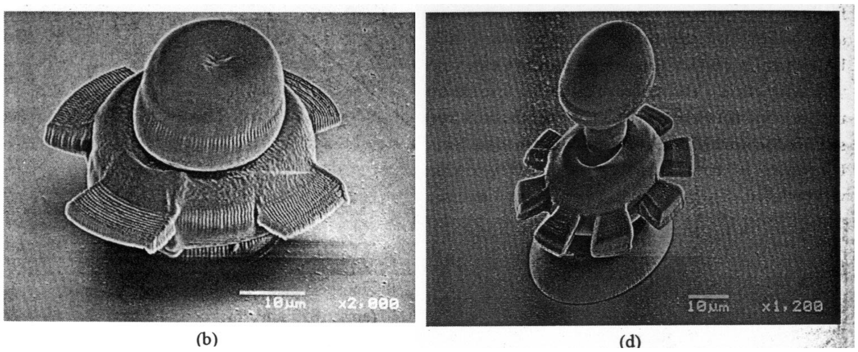

Fig. 10 Micro gear and shaft make of solidified polymer
(b) side view of the gear of four teeth
(d) side view of the gear of eight teeth

Micro Electro Mechanical Systems
Jan., 1998 Heidelberg, Germany

Combining Microstereolithography and Thick Resist UV Lithography

Combining Microstereolithography and Thick Resist UV Lithography for 3D Microfabrication

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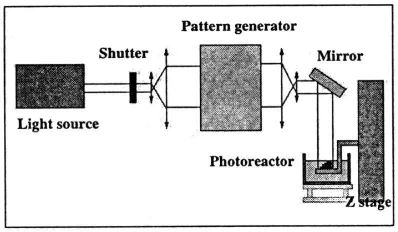

Fig. 1 Diagram of microstereolithorgraphy apparatus using a pattern generator.

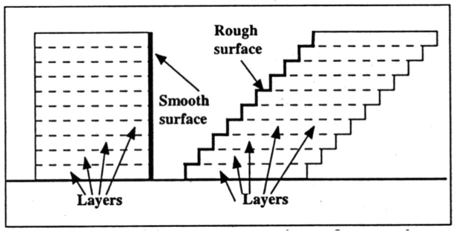

Fig. 2 Influence of the geometry on the surface roughness.

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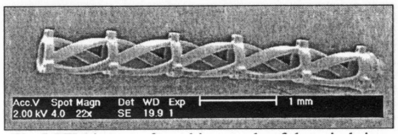

Fig. 5 SEM image of an object made of three imbricated springs. This structure consists of 1000 layers of 5µm each, built along the axis direction.

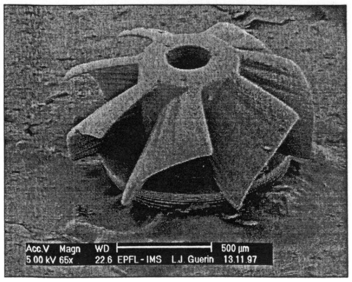

Fig. 4 WEM photograph of a micro-turbine made by microstereolithography.

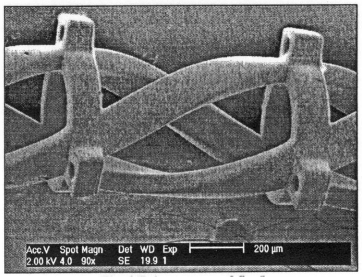

Fig. 6 Enlargement of fig. 5.

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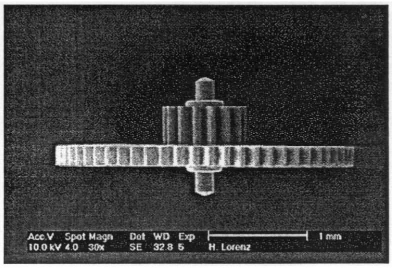

Fig. 11 Plastic injected watch gear, total height: 1.4 mm.

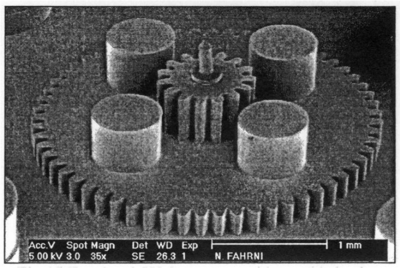

Fig. 15 Two level SU-8 structure with an added axle.

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