# **Micro-mirror Arrays for Maskless Lithography**

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## ABSTRACT

This paper presents a design approach for fabricating an array of MEMS mirrors suitable for maskless lithography applications in a commercial CMOS process. A small footprint mirror design is presented which uses a pair of support beams for signal routing and diagonal gap-closing actuators for mirror deflection. The actuators are shown to be capable of delivering up to 10nN of force per micron of actuator for a supply voltage of 30V, and 0.1nN per micron for a thick gate oxide 0.25µm CMOS supply voltage of 3.3V.

### **INTRODUCTION**

Maskless lithography has been proposed as a means to greatly reduce non-recurring engineering (NRE) costs in the fabrication of process generations future [1]. Maskless lithography entails the use of an integrated CMOS/MEMS microchip with an array of actuated mirrors and circuitry to transfer pattern data to a target wafer. Like a standard extreme ultraviolet (EUV) mask, the positive pattern is reflected onto the wafer (in this case, by mirrors in the "on" position). The negative pattern is reflected away by mirrors in the "off" position. To completely expose the wafer, the mask pattern will be electronically scrolled across the mirror array as the wafer is mechanically scanned under the focused pattern. Each pixel on the wafer is exposed by multiple mirrors, reducing the technique's sensitivity to MEMS device yield. Current maskless lithography research at U.C. Berkeley is targeted for a process with a 50 nanometer minimum feature size, approximately 3 process generations from the current leading 130nm process [2]. We developed a micro-mirror that meets the maskless constraints for a 0.25um process.

A micron-scale, flexure based MEMS mirror has been proposed in [1]. The limitation of the flexure design is "snap down": deflection is nonlinear and at about 1/3 of the gap, electrostatic forces will snap the mirror the remaining distance into contact with the base. Contact may result in wear, stiction, and charge accumulation. The flexure mirror avoids contact by just tilting enough to deflect the EUV beam away from the projection optics. In developing a physical model they assume that bending of the mirror is negligible all bending occurs at the 100nm hinge/support.



Figure 1. Micro-mirror layout

### DESIGN

The fabrication process used for our design was originally developed at Carnegie Mellon by Gary Fedder [3]. It is a CMOS compatible process with two post-processing steps. The first is an RIE etch of silicon dioxide down to either the first metal layer defined or the substrate. The second step is a wet etch of silicon dioxide. The wet etch releases metal structures that have been outlined by the RIE. An additional step is necessary beyond the normal Fedder process in which an EUV reflective layer is deposited on the mirror surfaces. This layer is described in [1], and we assume a process can be developed to deposit EUV reflective layers on our mirrors.

The Fedder process possesses several qualities which make it highly attractive for maskless lithography: small feature size, the capability for integrated electronics, and high yield. Small feature size is inherent because the process scales with CMOS technology. The semiconductor industry invests heavily in new process technology to scale CMOS. The Fedder process leverages that scaling. Maskless lithography requires integrated circuitry for mirror control. The process is also high yield, when compared to surface-micromachining postprocessing steps. Several hundred million mirrors are required for rapid maskless lithography. Yield will not be one hundred percent for such a large array, but as many mirrors as possible must be functional. However, because the Fedder process has a small number of post-processing steps, the yield is high, which reduces costs. One significant drawback to design of micro-mirror arrays in the Fedder process is the inability to stack released MEMS structures above CMOS circuitry. something made possible surface in micromachined approaches.



Figure 2. Cross section and wiring for out-ofplane actuation [4].

Methods for out-of-plane actuation compatible with the Fedder process have been demonstrated previously [4, 5]. The Fedder process is capable of producing multiple capacitors between comb fingers, as shown in figure 2. The three metal layers in the rotor are electrically connected. Metal-one and metal-three in the stator are separately connected. The configuration forms two sidewall capacitors. When a voltage is applied between the top or bottom capacitors, the rotor will shift vertically to minimize capacitance. The maximum displacement is a function of the vertical position that minimizes the activated sidewall capacitance. The out-of-plane actuation is not subject to snap down like the design in [1].

In [5], a torsion mirror is actuated by two out-of-plane comb drives. The stator comb fingers are defined by metal-three, metal-four, and metalfive. The mirror fingers are defined by metalthree. When a voltage is applied, the asymmetric comb drive creates an upward force on the mirror, causing it to rotate.

Our basic design consists of a  $5x5\mu m$  multi-layer square mirror (metal-one through metal-three, including underlying oxide layers), a

pair of single-layer support beams (metal-one and underlying oxide), and a multi-layer stator (metalone through metal-three, including underlying oxides) adjacent to one side of the mirror (figure 2). Mirror deflection is achieved by applying a voltage across pairs of diagonal gap-closing actuators (figure 3).



Figure 3. Cross section and applied voltages for outof-plane actuation.

The maskless lithography application requires a high mirror fill factor, meaning that the flexure must be small relative the mirror surface area, and a relatively square "footprint" for the combined mirror and support structure must be maintained. The support beams for our mirror are in an "antennae" configuration, anchored at the top of the mirror and turning backwards (Figure 1), in contrast to the single support design proposed in [1]. The use of antennae supports significantly increases the support beam length, while maintaining high fill factor for the mirror array. The spring constant of a support flexure is inversely proportional to the cube of the flexure's length, an effect which more than compensates for the additive effect of introducing two beams in parallel – by decreasing the support spring constants, greater out-of-plane actuation can be achieved for less force. The supports are connected to the mirror through a multi-layer backbone, and are made symmetric, in order to restrict the degrees of freedom. The antenna flexure has the lowest spring constant of the designs we considered that met our constraints.

We chose the signal routing to maximize the increase in capacitance when the mirror shifts upwards. In operation, an upward force is thus generated to reduce capacitance. The strength of the force is dependent on the change in capacitance with respect to vertical displacement z. The signal routing we designed is shown in figure 3. Metal layers in the mirror are oppositely charged with respect to the next highest metal layer in the stator. The resulting force, in seeking to minimize capacitance, lifts the mirror to reduce the distance between oppositely charged mirror and stator metal layers.

# **TEST STRUCTURES**

We designed the layout for six mirrors and other structures to test the micro-mirror concept. The structures meet lambda rules for the TSMC  $0.25\mu$ m process available through MOSIS. The first test mirror is our basic design. The mirror is topped by metal-three with etch-holes for release. The two flexures are metal-one to minimize beam thickness. One flexure carries high voltage to metal-one on the mirror and the other flexure grounds metal-two on the mirror. On the stator, metal-three is set to high voltage and metal-two is grounded. Thus electrostatic force is generated between metal layers of the mirror and stator. The second test mirror has flexures twice as long as the basic design to test the lower spring constant.

The third mirror tests poly flexures. If poly beams can be fabricated with the Fedder process, the flexures will lower the support spring constant, due to the decreased film thickness. Two mirrors test the minimum spacing between mirror and stator. Design rules dictate  $4\lambda$  minimum spacing between metal layers. The process may have some leeway beyond the design rules. One test mirror has  $3\lambda$  separation and one has  $2\lambda$ separation. The last two mirrors do not have a metal-three top. The "mirror" is just a metal-one and metal-two ring. If the undercut on the basic designs fail, the ring structures will likely be released.

We designed a structure with an out-ofplane actuation mechanism similar to the basic mirror design, but with a much higher capacitance. The structure has a long, comb-like interface between the stator and actuator. The capacitance is at least ten times that of the basic mirror design. Even if the capacitance of the basic design is not high enough to generate a discernible vertical deflection, this test structure will probably give results. We avoided the comb interface in our mirror design because it increases the size of the mirror and stator, reducing fill factor. The last set of structures will be used to test the Young's modulus of a laminated, metalone cantilever. The structures are simply three metal-one cantilevers of different lengths adjacent to a metal-two stator. We will use the resonant frequencies to characterize the beam structure for future redesigns.



Figure 4. Actuator force per micron length versus applied voltage.

### RESULTS

Because the complex geometry of the diagonal gap closing actuator precluded the development of a simple analytical expression for the actuator force, a simplified model was used. Each diagonal gap closing actuator was treated as a parallel plate capacitor, with the plate width taken as the thickness of the metal lines  $t_M$ , and the gap as the hypotenuse of the triangle formed by the planar separation between stator and actuator and the height of the stator. The resulting force per unit length for small deflection was found to be:

(1) 
$$F_e = \frac{N}{2} \frac{t_M (h-z)\varepsilon_0 V^2}{\left(d^2 + (h-z)^2\right)^{3/2}}$$

where z is the vertical deflection at the tip of the mirror, d is the planar gap between the mirror and stator, h is the combined thickness of two metal layers and the interlayer silicon dioxide, and N is the number of stacked actuators. As a reference, TSMC 0.25um capacitance tables show M1-M2 fringing fields of ~60aF/um, which correspond to roughly 9 aF/um fringing through air for one side of a metal line. Capacitance calculated from the above method yields 20.4 aF/um. A plot of expected zero deflection actuator force per micron length for a complete mirror (which includes two

actuating levels) versus applied voltage is shown in figure 4.

Mirror deflection angle can be approximated from the zero deflection actuator force and the resulting support beam bending profile:

(2) 
$$\theta = \tan^{-1} \left( \frac{F_e W L^2}{4EI} \right)$$

Results for a five micron wide mirror with five micron long support beams are shown in figure 5.

One basic requirement for the micromirror array is that it be able to switch at a rate faster than the pulse rate of the EUV laser (EUV lasers under development at the Lawrence Berkeley Laboratory currently operate at 10kHz). The expected resonant frequency of our designed mirror is several orders of magnitude larger, and calculated to be:

(3) 
$$f_0 = \frac{\sqrt{2k/m}}{2\pi} = 4.7 MHz$$

assuming a Young's modulus of around 70 GPa [3] and support beams five microns in length (with a calculated spring constant k=72.7 N/m).



Figure 5. Mirror angle as a function of applied voltage.

### CONCLUSION

A novel approach to high-yield fabrication of micro-mirror arrays for maskless lithography was presented. A diagonal gap-closing actuator was designed and characterized which could deliver up to 10nN of force per micron of actuator for a supply voltage of 30V (although only ~0.1nN for a thick gate oxide 0.25 $\mu$ m CMOS compatible supply voltage of 3.3V). Due to high

spring constants in the mirrors, however, the maximum deflection expected is on the order of hundredths of a degree.

#### REFERENCES

- N. Choksi, Y. Shroff, D. S. Pickard, Y. Chen, W. G. Oldham, M. McCord, R. F. W. Pease, D. Markle, "Maskless extreme ultraviolet lithography," *J. Vac. Sci. Technol. B* 17(6), Nov/Dec, 1999, pp. 3047-3051.
- [2] V. Dai, A. Zakhor, "Lossless Layout Compression for Maskless Lithography Systems," Proceedings of the SPIE Emerging Lithographic Technologies IV, vol 3997, March 2000.
- [3] G. K. Fedder, S. Santhanam, M. L. Reed, S.C. Eagle, D. F. Guillou, M. S.-C. Lu, and L. R. Carley, "Laminated High-Aspect-Ratio Microstructures Fabricated in a Conventional CMOS Process," *Sensors and Actuators A* 57, 103 – 110, 1996.
- [4] H. Xie and G. K. Fedder, "A CMOS-MEMS Lateral-axis Gyroscope," Proceedings of The 14th IEEE International Conference on Micro Electro Mechanical Systems (MEMS '01), January, 2001, pp. 162 - 165.
- [5] B. Warlick, "Design of a Microscale Torsion Mirror Fiber Optic Switch For Optical Internet Routers," Univerity of Virginia Undergraduate Thesis in Electrical Engineering, May 2001.



Figure 6. Test chip layout.