Today’s Lecture

- Overview: why is the E in MEMS important?
- Passive elements in integrated circuits: semiconductor basics, resistors, capacitors, and non-linear charge-storage elements
- Modeling a diffused resistor: successive approximations

- Reading:
  additional reference: EE 105 web site Fall 2003
  (A. M. Niknejad lecture notes)
Electronics for MEMS

- MEMS are the interface between the physical world and the digital electronic world
- Challenges (sensing)
  - Transduction often leads to small electrical signals
  - Dynamic range (max. signal / noise floor)
  - Temperature range for MEMS: automotive/military vs. consumer electronics
  - Extraneous inputs must be rejected
- Challenges (actuating)
  - MEMS-sized actuators have tiny mechanical power output … useful in arrays for steering photons, or for controlling other MEMS, or (someday) as elements in muscle-like distributed actuators

MEMS for Electronics

- Microstructures as frequency references or filters date to the pre-history of MEMS (circa 1965)
- Current interest:
  - High-frequency (10 MHz – 2 GHz) mechanical resonators for filters, mixers in cell phones and sensor networks
  - Thermal isolation structures for precision analog circuits
- Future:
  - Neural computation using coupled resonators
  - Optical interconnect MEMS mirrors
Bond Model for Silicon

Thermal Equilibrium (Pure Si)

- Balance between generation and recombination determines \( n_0 = p_0 \)
- **Strong** function of temperature

\[
n_i = \sqrt{N_c N_v e^{-E_i / 2kT}} = [1.71 \times 10^{19} \text{ cm}^{-3}] e^{-1.15 eV / 2kT}
\]

Room temperature (300 K)

\[
n_i = 1.45 \times 10^{10} \text{ cm}^{-3}
\]
Doping with Group V Elements

• P, As: extra bonding electron … lost to crystal at room temperature

Doping with Group III Elements

• Boron: 3 bonding electrons → one bond is unsaturated
Compensation

- Dope with both donors and acceptors

Carrier Concentrations with Doping

- Balance between generation and recombination:
  \[ n_o \cdot p_o = n_i^2 \]
  “mass-action law”

- Charge neutrality (bulk silicon away from surfaces):
  \[ 0 = q(p_o + N_d - N_a - n_o) = q\left(\frac{n_i^2}{n_o} + N_d - N_a - n_o\right) \]
  Assume n-type: \( N_d > N_a \)
Majority and Minority Carriers

- Ranges of doping concentrations in silicon:
  \[10^{13}\text{ cm}^{-3} < N_d, N_a < 5 \times 10^{19}\text{ cm}^{-3}\]
  
  must be located on substitutional lattice sites to be electrically active.

  Typical case: \(N_a \gg N_d\) or vice versa

Thermal Equilibrium

Rapid, random motion of holes and electrons at “thermal velocity” \(v_{th} = 10^7\text{ cm/s}\) with collisions every \(\tau_c = 10^{-13}\text{ s}\).

Apply an electric field \(E\) and charge carriers accelerate … for \(\tau_c\) seconds

\[\begin{array}{c}
\text{zero }E\text{ field} \\
\hline
v_a
\end{array}\]

\[\begin{array}{c}
\text{positive }E \\
\hline
v_a
\end{array}\]

(hole case)
Drift Velocity and Mobility

For holes:

\[ v_{dr} = a \cdot \tau_c = \left( \frac{F_e}{m_p} \right) c = \left( \frac{qE}{m_p} \right) c = \left( \frac{q\tau_c}{m_p} \right) E \]

\[ v_{dr} = \mu p E \]

For electrons:

Mobility vs. Doping in Silicon at 300 K

“default” values:
Mobility vs. Temperature in Silicon

Factor of 5 increase in electron mobility if temperature is dropped from 300 K to 40 K

Note: dopant activation begins to fall off below about 50 K.


EE C245 – ME C218 Fall 2003 Lecture 21

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Drift Current Density (Holes)

Hole case: drift velocity is in same direction as $E$

The hole drift current density is:

$$J_p^{dr} = q_p \mu_p E$$
Drift Current Density (Electrons)

Electron case: drift velocity is in opposite direction as $E$

$$J_n^{dr} = (-q) n \nu_{dn}$$

The electron drift current density is:

$$J_n^{dr} = (-q) n \nu_{dn}$$

units: Ccm$^{-2}$ s$^{-1}$ = Acm$^{-2}$

Resistivity

Bulk silicon: uniform doping concentration, away from surfaces

n-type example: in equilibrium, $n_o = N_d$.

When we apply an electric field, $n = N_d$.

$$J_n = q\mu_n nE = q\mu_n N_d E$$

Conductivity $\sigma_n$

Resistivity $\rho_n =$
Ohm’s Law

- Current $I$ in terms of $J_n$
- Voltage $V$ in terms of electric field

Sheet Resistance

- IC resistors have a specified thickness – not under the control of the circuit designer
- Eliminate $t$ by absorbing it into a new parameter: the sheet resistance

\[ R = \frac{\rho L}{Wt} = \left( \frac{\rho}{t} \right) \left( \frac{L}{W} \right) = R_{sq} \left( \frac{L}{W} \right) \]
Using Sheet Resistance

- Ion-implanted (or "diffused") IC resistor

Idealizations

- Why does current density $J_n$ "turn"?
- What is the thickness of the resistor?
- What is the effect of the contact regions?
IC Capacitors

Metal layers separated by insulators $\rightarrow$ get intentional (or parasitic) capacitor

$$C = \frac{\varepsilon d}{t_d}$$
Circuit Model

- Capacitance between metal 1 and metal 2:

$$C_{12} = \left( \frac{\varepsilon_d}{t_d} \right) A_{12}$$

- Other capacitors: what is terminal 3?

Surface Charge and Electric Field

- Diagram showing surface charge density and electric field.
pn Junction

- Ubiquitous in IC structures
Junction in Thermal Equilibrium

- Mobile electrons and holes can cross junction (huge concentration difference)
- Process creates balanced + and - charge layers because the donors and acceptors are “stuck” in the lattice and can’t move
- Limiting state with $V_D = 0$ V $\rightarrow$ thermal equilibrium
- “Built-in voltage” is about 1 V
Voltages in Thermal Equilibrium

Kirchhoff’s Voltage Law: where are the missing voltage drops?

Reverse Applied Bias ($V_D < 0$ V)

- Polarity increases charge stored in junction → increases barrier between p and n regions
- Current is negligible (due to high barrier)
Qualitative Charge-Voltage Plot

\[ Q_J = Q_{Jo} \sqrt{1 - \frac{V_D}{\Phi_B}} \]

Why isn't the plot linear?
Charge Storage in pn Junction

- Circuit element:

\[ i_D = dq/dt = (dq/dv)(dv/dt) \]

\[ q(V_D) \]

\[ V_D \]

- (Humans) can't handle non-linearity in KCL, KVL

Linearizing the Charge Storage

- Symbol conventions

\[ q_j = Q_j + q_j \]

\[ V_D = V_D + v_d \]
Diode Voltage $v_D(t)$

Incremental Charge $q_j$
Junction Capacitance $C_j$

- Slope of charge-voltage plot is the ratio of the small-signal charge to the small-signal voltage

$$slope = \frac{dq_j}{dv_D} \bigg|_{v_D} = \frac{q_j}{v_d}$$

- Define the slope (units: C/V = F) to be the junction capacitance $C_j$

The Diffused Resistor, Revisited

pn junction under reverse bias (we hope!)