Technology for the MEMS processing and testing environment

SUSS MicroTec AG
Dr. Hans-Georg Kapitza
SUSS MicroTec Industrial Group

Founded 1949 as Karl Süss KG GmbH&Co. in Garching/ Munich

Worldwide 13 companies

Sales & Service Center

Vaihingen, Asslar, Dresden, Munich, St. Jeoire, San Jose, Phoenix, Waterbury, London, Shanghai, Hsinchu, Bangkok, Yokohama, Shanghai
SUSS MicroTec Semi Markets

- Micro System Technologies / Optronics
  Sensors, Actuators,
  Micro-optical components

- Advanced Packaging -
  Chip Connection

- Compound Semiconductor
  III-V as GaAs, also GeOI, GeOSi...

- Test & Measurement
  IC-Development, Quality Assurance
SUSS MicroTec: Product Portfolio

Mask Aligner (Lithography)  70% of SUSS MicroTec Sales  Spin Coater and Developer Cluster Tools
SUSS MicroTec: Product Portfolio

Substrate Bonder

Device Bonder

Prober (Test & Measurement)
SUSS enables Process transfer – from Development to Production

• Production Technologies for MEMS – Overview

...Industrial Production

Lab / Small Scale Production...
Production Technologies for MEMS – Overview

Typical MEMS - Process

- Lift-off Tools
- Anodic / Thermo-kompression Bonder
- Low Temp Fusion Bonder nanoPrep
- Mounting / Dicing
- Wafer Level Packaging
- Inspection / Testing
- Substrate Bonding
- Etching / Metal Deposition
- Thermal Treatment / Lift-Off
- Topography Coating & Lithography
- Cleaning, dehydration bake
- Spin Coater
- Spray Coater
- Mask Aligner
- Developer
- Spin Coater Technology
- SupraYield Technology
- nanoPrep
- Device Bonder
- MEMUNITY
- The MEMS Test Community

Produktionssysteme in der Mikrosystemtechnik 2003 7
Coating of Photoresist - The Spin Coating Technology

The photolithographic process begins by spreading photosensitive material, called photoresist, evenly over the wafer surface.

Here the **spin coating** is the current state-of-the-art technology:
Spin Coating of Topographic Structures

Spin coating leads to poor coverage of edges and spin shadowing on MEMS-typical structured substrates ⇔ Need for **new coating technology**
Spray Coating I

- Clariant AZ5214E modified
- V-grooved Wafer
- Groove depth 150µm

Layer thickness ca. 8µm

Layer thickness ca. 4µm
**Spray Coating II**

Details of convex and concave transitions

- **Clariant AZ5214E modified**

![Spray Coating Images](image-url)
• Photolithography – Photoresist Coating

Spray Coating - Trench
Patterning of MEMS-Typical Thick Photoresist Layers

Projection Printing used by steppers vs. Proximity Printing used by mask aligners (simplified principle)
Exposing Pattern Into Photoresist

Patterns are imaged from a **mask** to a coated wafer and exposed into the resist.
# Exposing Pattern Into Photoresist

Resolution capabilities of SUSS Mask Aligners

<table>
<thead>
<tr>
<th>Resolution</th>
<th>UV250 4” wafer</th>
<th>UV400 4” wafer</th>
<th>UV400 6” wafer</th>
<th>4” wafer</th>
<th>6” wafer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proximity (20 µm gap)</td>
<td>&lt;3.0µm</td>
<td>&lt;3.0µm</td>
<td>&lt;3.0µm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Soft Contact</td>
<td>&lt; 2.5µm</td>
<td>&lt; 2.5µm</td>
<td>&lt;2.0µm</td>
<td>&lt; 0.8µm</td>
<td>&lt; 0.8µm</td>
</tr>
<tr>
<td>Hard Contact</td>
<td>&lt;2.0µm</td>
<td>&lt;2.0µm</td>
<td>&lt; 2.0µm</td>
<td>&lt;1.0µm</td>
<td>&lt;1.0µm</td>
</tr>
<tr>
<td>Vacuum Contact</td>
<td>&lt;0.8µm</td>
<td>&lt;0.8µm</td>
<td>&lt; 1.0µm</td>
<td>&lt;0.4µm</td>
<td>&lt;1.0µm</td>
</tr>
</tbody>
</table>

Resolution achieved in Hoechst AZ1512 Resist (UV400 and UV300)
Resolution achieved in Shipley UV VI (UV250 optics) on 4” and 6” Si-wafers, (1 µm thick resist, lines & spaces)
Strengths of Mask Aligners:
- Structures < 1 µm (0.5µm)
- Large depth of focus
- Resist thickness 1 - 50µm
- Top and back side alignment
- Overlay accuracy better 1 µm

The production of future MEMS require further enhancement of patterning technology
SupraYield: Applications for Lithography

- NG-Litho
- Stepper / Scanner
- Mask Aligner
- Screen Printing

Integrated Circuits
Thin Film Heads

High Res Stepper

Low Res Stepper

3 D – UV Lithography
MEMS
Adv. Packaging
MCM
(Intel BBUL)

PCBs

Resolution

0.1 µm
1.0 µm
10 µm
100 µm

Low Cost Aligner

Mask Aligner

Low Res Stepper
SupraYield: Applications for Lithography

- SupraYield: High Res Stepper Technology
- NG-Litho
- Stepper / Scanner
- Mask Aligner
- Screen Printing

- Integrated Circuits
  - Thin Film Heads
  - SUSS SupraYield Technology

- 3 D - UV Lithography
  - MEMS
  - Adv. Packaging
  - MCM (Intel BBUL)

- 0.1 µm to 100 µm Resolution

PCBs

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Mask Aligner / Contact Printing - Problem and Solution

Contact Printing

Proximity Printing

Photolithography – Patterning
The Problem

- Production Vacuum Contact Printing
  - Mask Sticking To Wafer
  - Resist Pulled From Wafer Onto Mask
    - Damaged Resist Can Not be Image properly
    - Particles Do not allow Close Contact
    - Particles Image As Defects

- Causing
  - Mask Cleaning Required Every Few Wafers
  - Lower Throughput
  - Higher Defect Level

0.75 µm lines and spaces
(at first print and eighth print)
**SUSS SupraYield Technology**

- **Mask protection agent**
  - Applied to Chrome Side of Mask
  - Optically Transparent
  - Low Surface Tension
  - Non-Stick

- **Mask protection agent makes wafer release much easier**
  - No sticking to the mask

- **Mask protection agent repels and removes particles of all kinds**
  - No resist build-up
Result of SUSS - SupraYield Technology

1000 Exposures 0.75µm Lines & Spaces

Without any Mask Cleaning

Photolithography – Patterning
nanoPREP: Direct Wafer Bonding

Direct Wafer Bonding is utilized in:

- Silicon on Silicon-Oxide: *Silicon on Insulator (SOI)*
- Silicon-Germanium on Silicon: *Strained Silicon (sSOI)* (high electron mobility, fast ICs)

**Direct bonded wafers that require Low Temperature Annealing (< 350°C):**

- All wafers which already embody semiconductor components (CMOS structures)
  - MEMS production
    - Connection of sensors and analytical levels (MEMS meets CMOS)
  - MEMS packaging
    - Micro mirror displays (DLP)
    - Hermetically sealed sensors
nanoPREP: Direct Wafer Bonding

The Challenge:

- **Faultless Direct Wafer Bonding at low temperatures (<350°C) requires:**
  - Elimination of organic contamination
  - Molecular surface activation
  - Instant fusion of the wafers after the activation
nanoPREP: Ambient Pressure Plasma Activation

The Solution:

- Plasma Activation for Low Temperature Annealing for Direct Wafer Bonding
  - Ambient pressure plasma activation
  - No vacuum required
  - SUSS MicroTec patent pending – no violation of SiGen patent
  - Automatic cluster solution allows controlled process times

[Diagram of plasma activation setup with labels: High voltage, Oscillatory movement, Grounded substrate table, Gas gap filled with micro discharges, Wafer, HV electrodes with ceramic isolation, Gas shower]
Fusion Bonding - Plasma Activation

MHU module + CL200 module(s) + IR Inspection module(s)

= Fusion Bonder Cluster
+ AP Plasma Activation module(s)
Fusion Bonder Cluster for MEMS

MEMS cluster:
- I/O ports
- I/O MHU
- process MHU(s)
- Fusion Bonder mModule(s)
  - Plasma Activation
  - Cleaning
  - Bonding
- IR-inspection module
Probing for MEMS

Technical Solutions:

- Semiautomatic vacuum prober systems e.g. PAV 150
- Wafer chucks for Pressure Calibration (air stream)
- Acceleration chucks
- Full wafer pressure test chamber 1 mbar ... 50 bar, humidity control 0...85% RH, from – 40°... +160° C at an pressure accuracy better 0.1% ! (DELTA)